

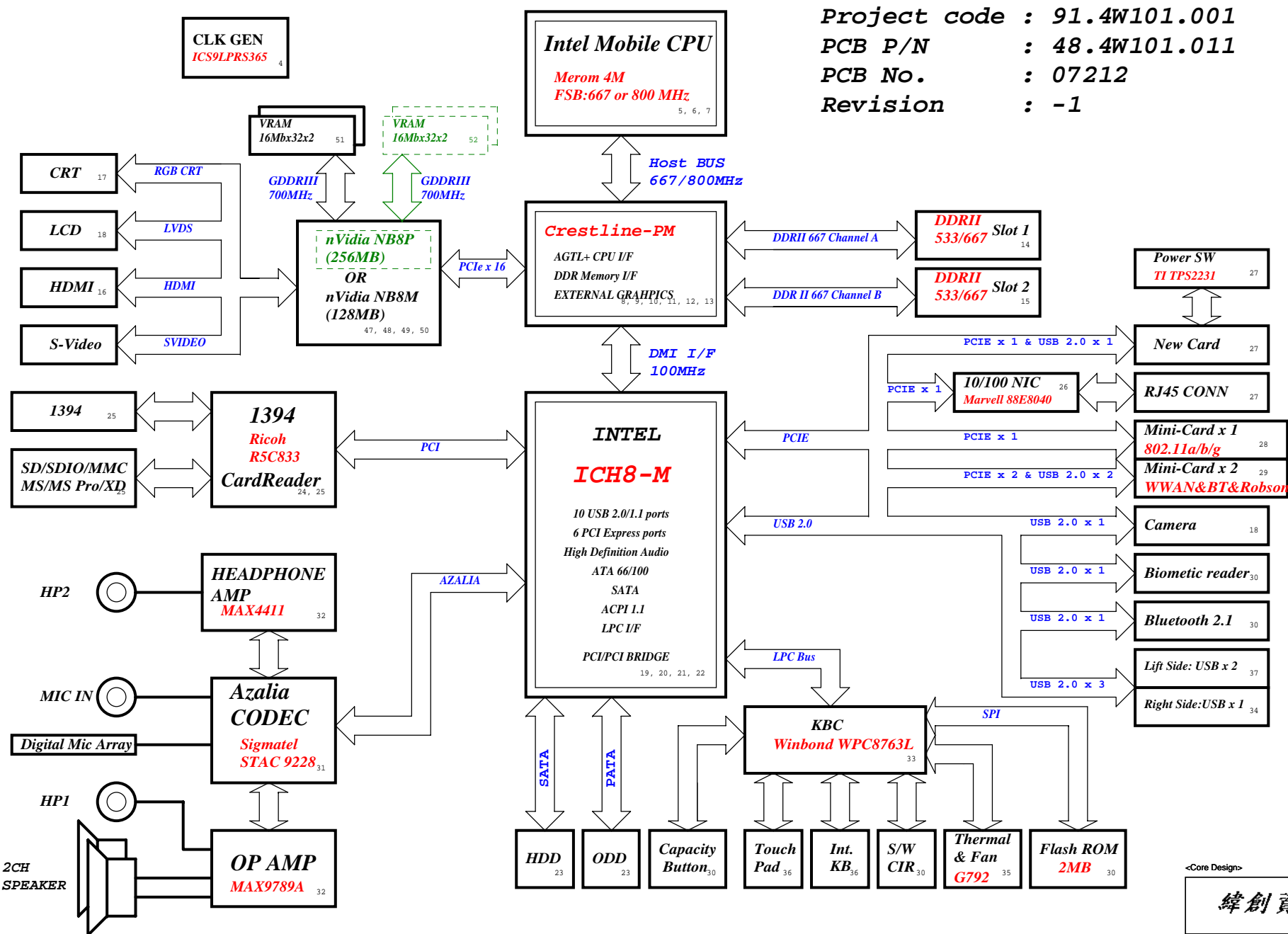
Hawke Intel Discrete Block Diagram

Project code : 91.4W101.001

PCB P/N : 48.4W101.011

PCB No. : 07212

Revision : -1



BATTERY CHARGER	
MAX8731A 38	
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT
SYSTEM DC/DC	
TPS51120 39	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
SYSTEM DC/DC	
TPS5117 42, 43	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
SYSTEM DC/DC	
TPS51100 44	
INPUTS	OUTPUTS
1D8V_S3	0D9V_S3
SYSTEM DC/DC	
RT9018 44	
INPUTS	OUTPUTS
1D8V_S3 1D8V_S3	1D5V_S0 1D25V_S0
VGA DC/DC	
TPS5117 53	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFX_CORE_S0
CPU DC/DC	
ISL6262A 40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
PCB LAYER	
L1:TOP	
L2:GND	
L3:Signal	
L4:Signal	
L5:VCC	
L6:Singal	
L7:GND	
L8:BOT	

<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

	Title
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System Block Diagram

Size
A3

Document Number

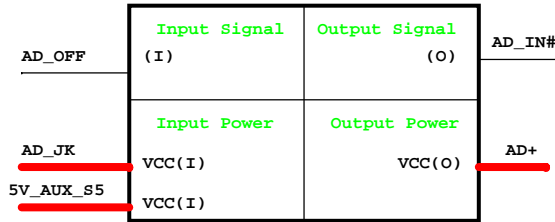
Hawke-Intel

Rev

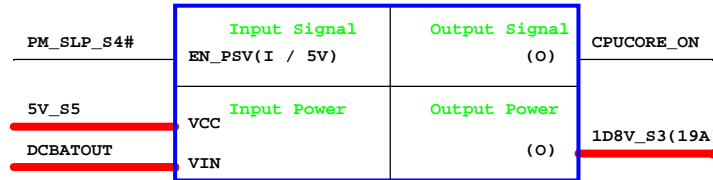
Date: Sunday, September 09, 2007

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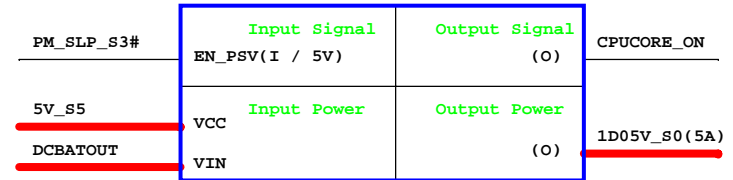
Adapter



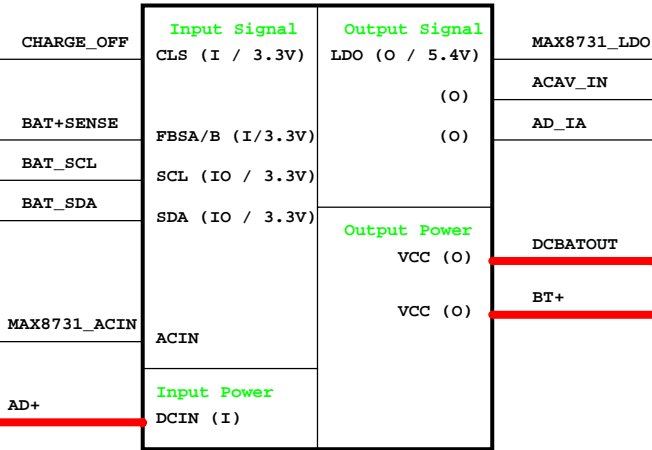
TPS51117 1D8V



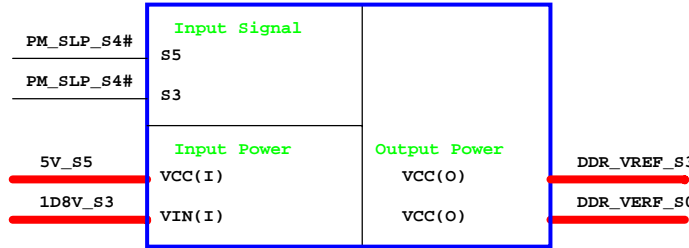
TPS51117 1D05V



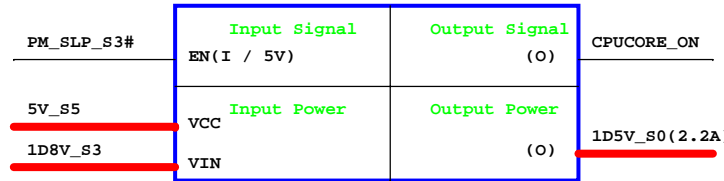
Charger MAX8731A



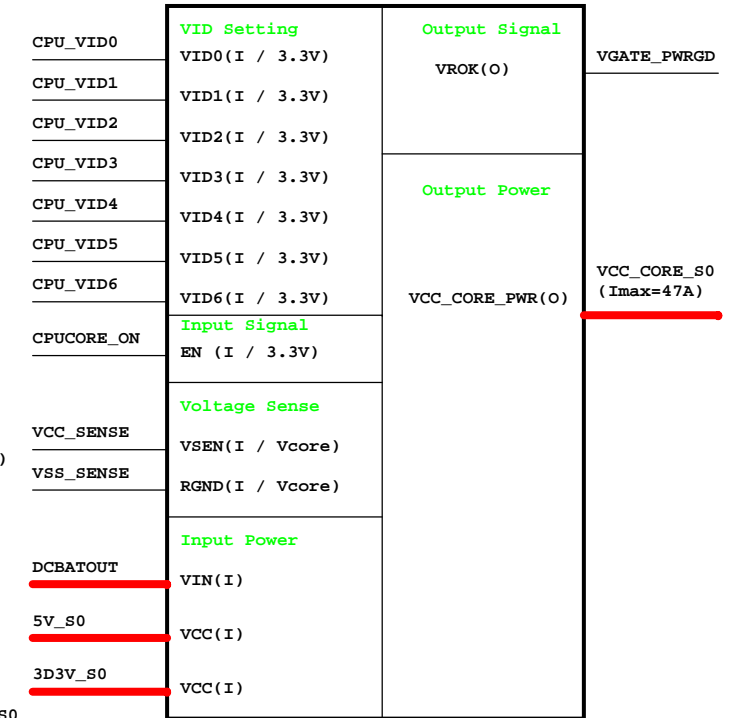
TI TPS51100 0.9V/DDR_VREF_S3



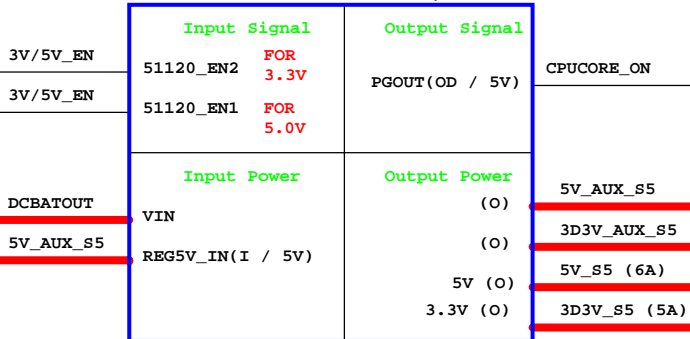
RT9018A 1D5V



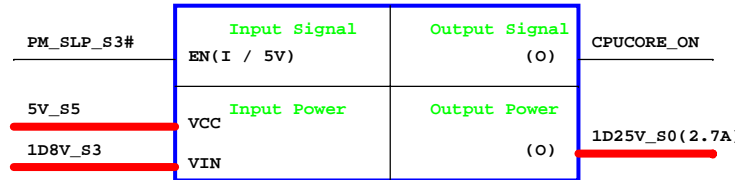
ISL6262A CPU_CORE



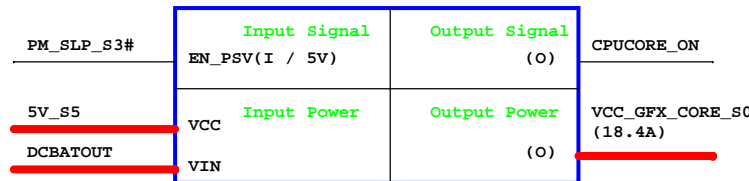
TI TPS51120 3D3V/5V



RT9018A 1D25V



TPS51117 VGA_CORE



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INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWB BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
ICH_RSVP	TP3	AZ_DOUT	ICH
0	0	1	RSVD
0	1	1	Enter XOR Chain
1	0	0	Normal Operation(default)
1	1	1	Set PCIE port cofig bit1

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable	
	high = default	
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

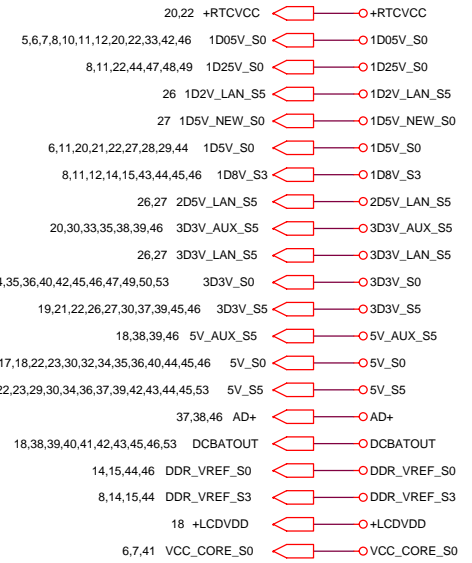
8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present
CFG 12 CFG 13	XOR/ALL-Z	
LL(00)	Reserved	
LH(01)	XOR Mode Enabled	
HL(10)	All Z Mode Enabled	
HH(11)	Normal Operation	



PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A D	0	0

USB TABLE

USB0	Ext Lift Side (Bottom)
USB1	Ext Lift Side (Top)
USB2	Ext Right Side
USB3	N/A
USB4	WWAN
USB5	Bluetooth
USB6	Camera
USB7	Biometric
USB8	Express Card
USB9	3rd mini card

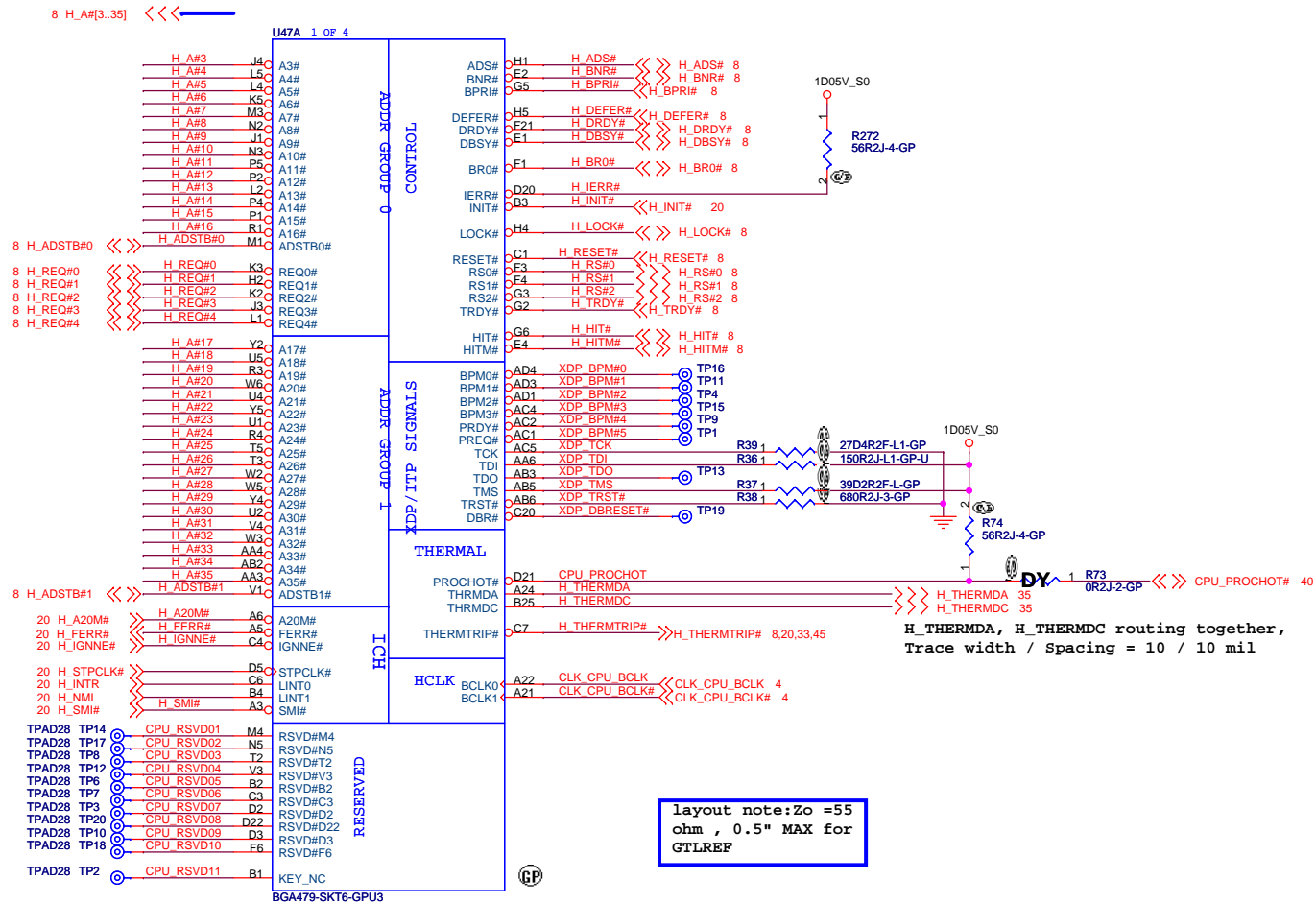
PCIE Routing

LANE1	10/100M Bit LOM
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN
LANE4	BT/UWB/Robson
LANE5	Express Card
LANE6	N/A

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Main source : 62.10079.021 Tyco 2-1871873-4
2nd source : 62.10040.221 Foxconn PZ47827-274M-41

<Core Design>

8 H_D#0[0.63] <<>>

8 H_DSTBN#0
8 H_DSTBP#0
8 H_DINV#0

8 H_DSTBN#1
8 H_DSTBP#1
8 H_DINV#1

4.8 CPU_BSEL0
4.8 CPU_BSEL1
4.8 CPU_BSEL2

PLACE C617 close to the TEST4 PIN,
make sure TEST3,TEST4,TEST5 trace
routing is reference to GND and
away other noisy signals

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

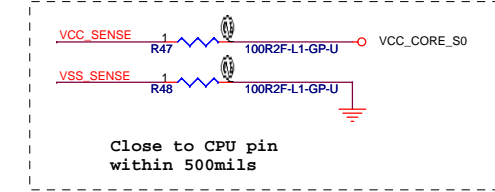
Resistor Placed
within 0.5" of CPU
pin. Trace should
be at least 25 mils
away from any other
toggling signal .
COMP[0,2] trace
width is 18 mils.
COMP[1,3] trace
width is 4 mils .

VCC_CORE_S0

VCC_CORE_S0

layout note:
place C618 near
PIN B26

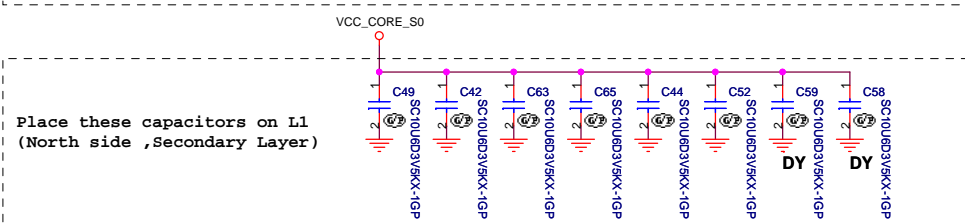
Length match within
25 mils . The trace
width/space/other is
20/7/25 .



<Core Design>

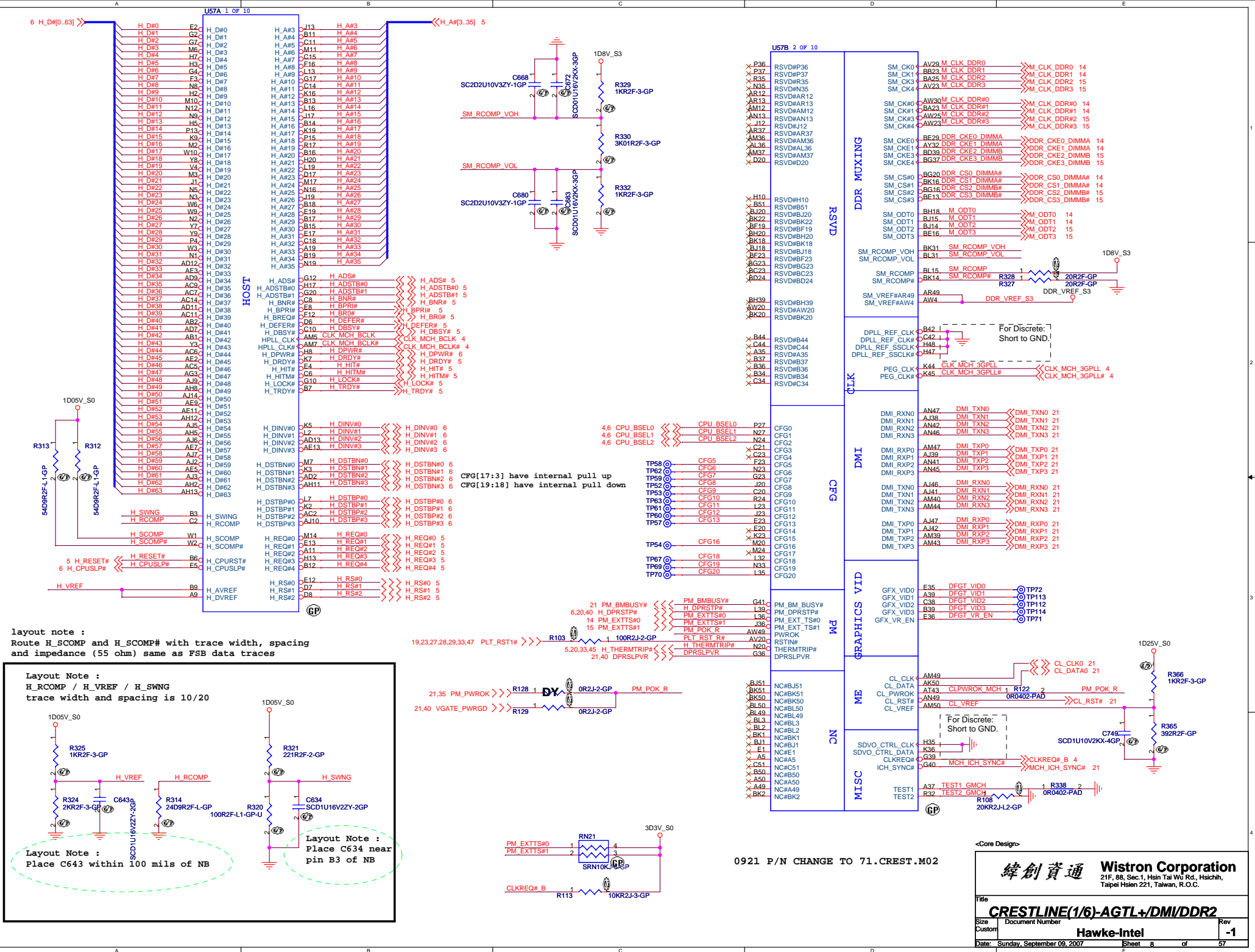
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Title			Rev
Meron(2/3)-AGTL+PWR			
Size	Document Number	Rev	
A3		-1	
Date:	Sunday, September 09, 2007	Sheet	6 of 57



Mid Frequncd Decoupling





<< >> DDR_A_D[0..63] 14
>>> DDR_A_BS[0..2] 14
>>> DDR_A_DM[0..7] 14
<< >> DDR_A_DQS[0..7] 14
<< >> DDR_A_DQS#[0..7] 14
>>> DDR_A_MA[0..14] 14

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DDR A D0	AR43	SA_DQ0	SA_BS0	BB19	DDR A BS0
DDR A D1	AW44	SA_DQ1	SA_BS1	BK19	DDR A BS1
DDR A D2	BA45	SA_DQ2	SA_BS2	BF29	DDR A BS2
DDR A D3	AY46	SA_DQ3			
DDR A D4	AR41	SA_DQ4	SA_CAS#	BL17	DDR A CAS#
DDR A D5	AR45	SA_DQ5		>>>	DDR_A_CAS# 14
DDR A D6	AT42	SA_DQ6	SA_DM0	AT45	DDR A DM0
DDR A D7	AW47	SA_DQ7	SA_DM1	BD44	DDR A DM1
DDR A D8	BB45	SA_DQ8	SA_DM2	BD42	DDR A DM2
DDR A D9	BF48	SA_DQ9	SA_DM3	AW38	DDR A DM3
DDR A D10	BG47	SA_DQ10	SA_DM4	AW13	DDR A DM4
DDR A D11	BJ45	SA_DQ11	SA_DM5	BG8	DDR A DM5
DDR A D12	BB47	SA_DQ12	SA_DM6	AY5	DDR A DM6
DDR A D13	BG50	SA_DQ13	SA_DM7	AN6	DDR A DM7
DDR A D14	BH49	SA_DQ14			
DDR A D15	BE45	SA_DQ15	SA_DQS0	AT46	DDR A DQS0
DDR A D16	AW43	SA_DQ16	SA_DQS1	BE48	DDR A DQS1
DDR A D17	BE44	SA_DQ17	SA_DQS2	BB43	DDR A DQS2
DDR A D18	BG42	SA_DQ18	SA_DQS3	BC37	DDR A DQS3
DDR A D19	BE40	SA_DQ19	SA_DQS4	BB16	DDR A DQS4
DDR A D20	BF44	SA_DQ20	SA_DQS5	BH6	DDR A DQS5
DDR A D21	BH45	SA_DQ21	SA_DQS6	BB2	DDR A DQS6
DDR A D22	BG40	SA_DQ22	SA_DQS7	AP3	DDR A DQS7
DDR A D23	BE40	SA_DQ23	SA_DQS#0	AT47	DDR A DQS#0
DDR A D24	AR40	SA_DQ24	SA_DQS#1	BD47	DDR A DQS#1
DDR A D25	AW40	SA_DQ25	SA_DQS#2	BC41	DDR A DQS#2
DDR A D26	AT39	SA_DQ26	SA_DQS#3	BA37	DDR A DQS#3
DDR A D27	AW36	SA_DQ27	SA_DQS#4	BA16	DDR A DQS#4
DDR A D28	AW41	SA_DQ28	SA_DQS#5	BH7	DDR A DQS#5
DDR A D29	AY41	SA_DQ29	SA_DQS#6	BC1	DDR A DQS#6
DDR A D30	AV38	SA_DQ30	SA_DQS#7	AP2	DDR A DQS#7
DDR A D31	AT38	SA_DQ31			
DDR A D32	AV13	SA_DQ32	SA_MA0	BJ19	DDR A MA0
DDR A D33	AT13	SA_DQ33	SA_MA1	BD20	DDR A MA1
DDR A D34	AW11	SA_DQ34	SA_MA2	BK27	DDR A MA2
DDR A D35	AV11	SA_DQ35	SA_MA3	BH28	DDR A MA3
DDR A D36	AU15	SA_DQ36	SA_MA4	BL24	DDR A MA4
DDR A D37	AT11	SA_DQ37	SA_MA5	BK28	DDR A MA5
DDR A D38	BA13	SA_DQ38	SA_MA6	BJ27	DDR A MA6
DDR A D39	BA11	SA_DQ39	SA_MA7	BJ25	DDR A MA7
DDR A D40	BE10	SA_DQ40	SA_MA8	BL28	DDR A MA8
DDR A D41	BD10	SA_DQ41	SA_MA9	BA28	DDR A MA9
DDR A D42	BD8	SA_DQ42	SA_MA10	BC19	DDR A MA10
DDR A D43	AY9	SA_DQ43	SA_MA11	BE28	DDR A MA11
DDR A D44	BG10	SA_DQ44	SA_MA12	BG30	DDR A MA12
DDR A D45	AW9	SA_DQ45	SA_MA13	BJ16	DDR A MA13
DDR A D46	BD7	SA_DQ46	SA_MA14	BJ29	DDR A MA14
DDR A D47	BB9	SA_DQ47			
DDR A D48	BB5	SA_DQ48	SA_RAS#	BE18	DDR A RAS#
DDR A D49	AY7	SA_DQ49	SA_RCVEN#	AY20	SA_RCVEN#
DDR A D50	AT5	SA_DQ50		>>>	DDR_A_RAS# 14
DDR A D51	AT7	SA_DQ51	SA_WE#	BA19	DDR A WE#
DDR A D52	AY6	SA_DQ52		>>>	DDR_A_WE# 14
DDR A D53	BB7	SA_DQ53			
DDR A D54	AR5	SA_DQ54			
DDR A D55	AR5	SA_DQ55			
DDR A D56	AR9	SA_DQ56			
DDR A D57	AN3	SA_DQ57			
DDR A D58	AM8	SA_DQ58			
DDR A D59	AN10	SA_DQ59			
DDR A D60	AT9	SA_DQ60			
DDR A D61	AN9	SA_DQ61			
DDR A D62	AM9	SA_DQ62			
DDR A D63	AN11	SA_DQ63			

DDR SYSTEM MEMORY A



<< >> DDR_B_D[0..63] 15
>>> DDR_B_BS[0..2] 15
>>> DDR_B_DM[0..7] 15
<< >> DDR_B_DQS[0..7] 15
<< >> DDR_B_DQS#[0..7] 15
>>> DDR_B_MA[0..14] 15

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DDR B D0	AP49	SB_DQ0	SB_BS0	AY17	DDR B BS0
DDR B D1	AR51	SB_DQ1	SB_BS1	BG18	DDR B BS1
DDR B D2	AW50	SB_DQ2	SB_BS2	BG36	DDR B BS2
DDR B D3	AW51	SB_DQ3			
DDR B D4	AN51	SB_DQ4	SB_CAS#	BE17	DDR B CAS#
DDR B D5	AN50	SB_DQ5		>>>	DDR_B_CAS# 15
DDR B D6	AV50	SB_DQ6	SB_DM0	AR50	DDR B DM0
DDR B D7	AV49	SB_DQ7	SB_DM1	BD49	DDR B DM1
DDR B D8	BA50	SB_DQ8	SB_DM2	BK45	DDR B DM2
DDR B D9	BB50	SB_DQ9	SB_DM3	BL39	DDR B DM3
DDR B D10	BA49	SB_DQ10	SB_DM4	BH12	DDR B DM4
DDR B D11	BE50	SB_DQ11	SB_DM5	BJ7	DDR B DM5
DDR B D12	BA51	SB_DQ12	SB_DM6	BF3	DDR B DM6
DDR B D13	AY49	SB_DQ13	SB_DM7	AW2	DDR B DM7
DDR B D14	BE50	SB_DQ14			
DDR B D15	BF49	SB_DQ15	SB_DQS0	AT50	DDR B DQS0
DDR B D16	BJ44	SB_DQ16	SB_DQS1	BD50	DDR B DQS1
DDR B D17	BJ44	SB_DQ17	SB_DQS2	BK46	DDR B DQS2
DDR B D18	BJ43	SB_DQ18	SB_DQS3	BK39	DDR B DQS3
DDR B D19	BL43	SB_DQ19	SB_DQS4	BJ12	DDR B DQS4
DDR B D20	BK47	SB_DQ20	SB_DQS5	BL7	DDR B DQS5
DDR B D21	BK49	SB_DQ21	SB_DQS6	BE2	DDR B DQS6
DDR B D22	BK43	SB_DQ22	SB_DQS7	AV2	DDR B DQS7
DDR B D23	BK42	SB_DQ23	SB_DQS#0	AU50	DDR B DQS#0
DDR B D24	BJ41	SB_DQ24	SB_DQS#1	BC50	DDR B DQS#1
DDR B D25	BL41	SB_DQ25	SB_DQS#2	BL45	DDR B DQS#2
DDR B D26	BJ37	SB_DQ26	SB_DQS#3	BK38	DDR B DQS#3
DDR B D27	BJ36	SB_DQ27	SB_DQS#4	BK12	DDR B DQS#4
DDR B D28	BK41	SB_DQ28	SB_DQS#5	BK7	DDR B DQS#5
DDR B D29	BJ40	SB_DQ29	SB_DQS#6	BE2	DDR B DQS#6
DDR B D30	BL35	SB_DQ30	SB_DQS#7	AV3	DDR B DQS#7
DDR B D31	BK37	SB_DQ31			
DDR B D32	BK13	SB_DQ32	SB_MA0	BC18	DDR B MA0
DDR B D33	BE11	SB_DQ33	SB_MA1	BG28	DDR B MA1
DDR B D34	BK11	SB_DQ34	SB_MA2	BG25	DDR B MA2
DDR B D35	BC11	SB_DQ35	SB_MA3	AW17	DDR B MA3
DDR B D36	BC13	SB_DQ36	SB_MA4	BE25	DDR B MA4
DDR B D37	BE12	SB_DQ37	SB_MA5	BE25	DDR B MA5
DDR B D38	BC12	SB_DQ38	SB_MA6	BA29	DDR B MA6
DDR B D39	BG12	SB_DQ39	SB_MA7	BC28	DDR B MA7
DDR B D40	BJ10	SB_DQ40	SB_MA8	AY28	DDR B MA8
DDR B D41	BL9	SB_DQ41	SB_MA9	BD37	DDR B MA9
DDR B D42	BL5	SB_DQ42	SB_MA10	BG17	DDR B MA10
DDR B D43	BK5	SB_DQ43	SB_MA11	BE37	DDR B MA11
DDR B D44	BK9	SB_DQ44	SB_MA12	BA39	DDR B MA12
DDR B D45	BK10	SB_DQ45	SB_MA13	BG13	DDR B MA13
DDR B D46	BJ8	SB_DQ46	SB_MA14	BE24	DDR B MA14
DDR B D47	BJ6	SB_DQ47			
DDR B D48	BE4	SB_DQ48	SB_RAS#	AV16	DDR B RAS#
DDR B D49	BH5	SB_DQ49	SB_RCVEN#	AY18	SB_RCVEN#
DDR B D50	BG1	SB_DQ50		>>>	DDR_B_RAS# 15
DDR B D51	BC2	SB_DQ51	SB_WE#	BC17	DDR B WE#
DDR B D52	BK3	SB_DQ52		>>>	DDR_B_WE# 15
DDR B D53	BE4	SB_DQ53			
DDR B D54	BJ2	SB_DQ54			
DDR B D55	BJ2	SB_DQ55			
DDR B D56	BA3	SB_DQ56			
DDR B D57	BB3	SB_DQ57			
DDR B D58	AR1	SB_DQ58			
DDR B D59	AT3	SB_DQ59			
DDR B D60	AY2	SB_DQ60			
DDR B D61	AY3	SB_DQ61			
DDR B D62	AU2	SB_DQ62			
DDR B D63	AT2	SB_DQ63			

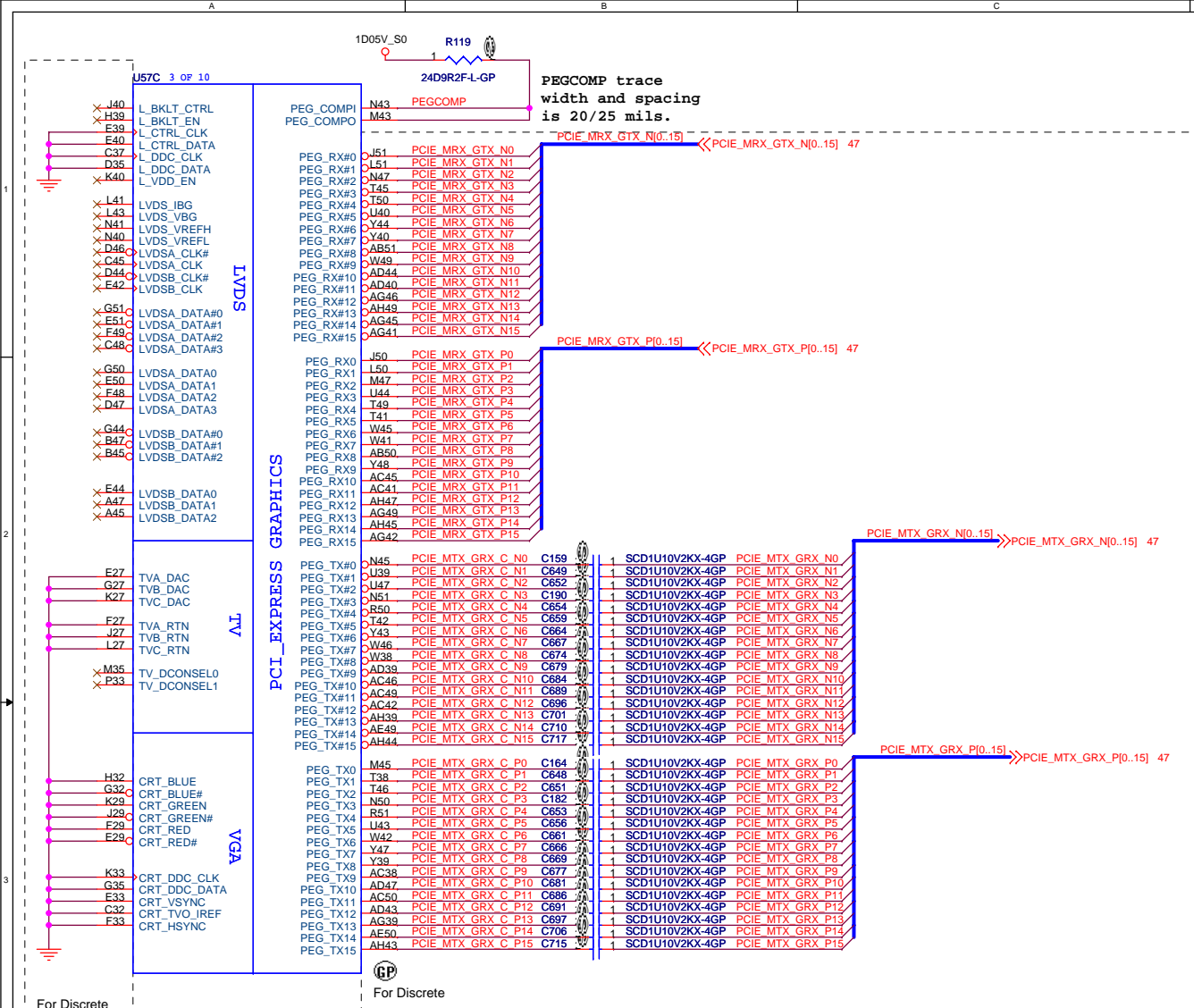
DDR SYSTEM MEMORY B



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
CRESTLINE(2/6)-DDR2 A/B CH
Size A3 Document Number Hawke-Intel Rev -1
Date: Sunday, September 09, 2007 Sheet 9 of 57



Strap Pin Table

CFG[2:0] FSB Freq select

CFG5 (DMI select)

CFG6

CFG7 (CPU Strap)

CFG8 (Low power PCIE)

CFG9
(PCIE Graphics Lane Reversal)

CFG[11:10]

CFG[13:12] (XOR/ALLZ)

CFG[15:14]

CFG16 (FSB Dynamic ODT)

CFG[18:17]

SDVO_CTRLDATA

CFG19(DMI Lane Reversal)

CFG20(PCIE/SDVO consurrent)

010 = FSB 800MHz
011 = FSB 667MHz
Others = Reserved

0 = DMI x 2
1 = DMI x 4 *

Reserved

0 = Reserved
1 = Mobile CPU *

0 = Normal mode
1 = Low Power mode *

0 = Reverse Lane
1 = Normal Operation *

Reserved

00 = Reserved
01 = XOR Mode Enabled
10 = All Z Mode Enabled
11 = Normal Operation (Default)*

Reserved

0 = Disable
1 = Enable *

Reversed

0 = No SDVO Device Present *
1 = SDVO Device Present

0 = Normal Operation
(Lane number in Order)
1 = Reverse lane

0 = Only PCIE or SDVO is operational *
1 = PCIE/SDVO are operating simu.

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRESTLINE(3/6)-VGA/LVDS/TV

Size
A3

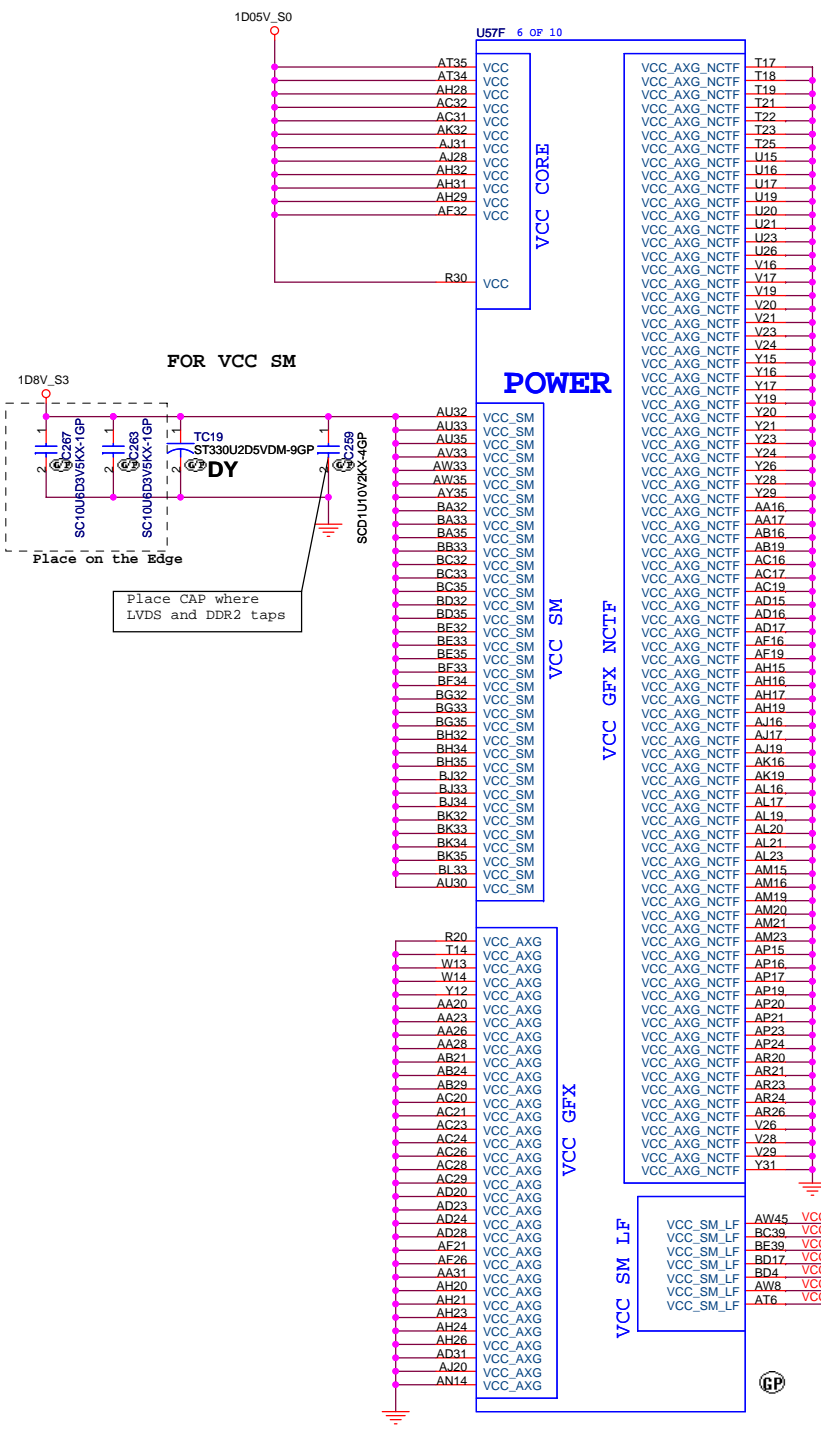
Document Number

Hawke-Intel

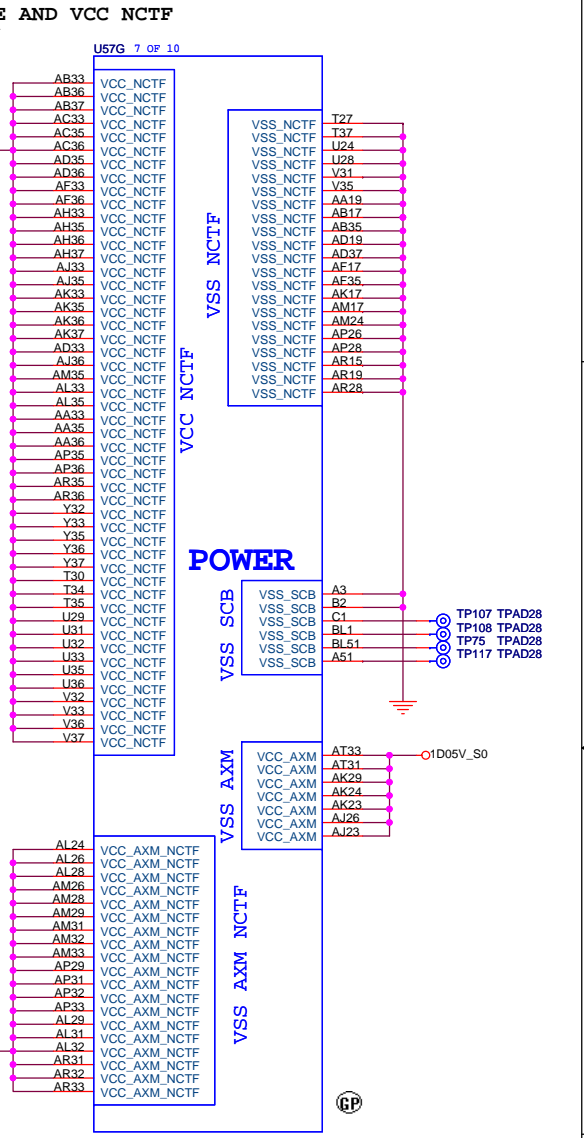
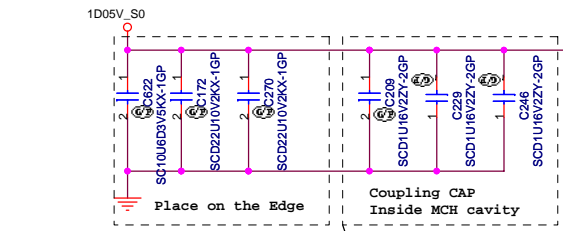
Rev
-1

Date: Sunday, September 09, 2007

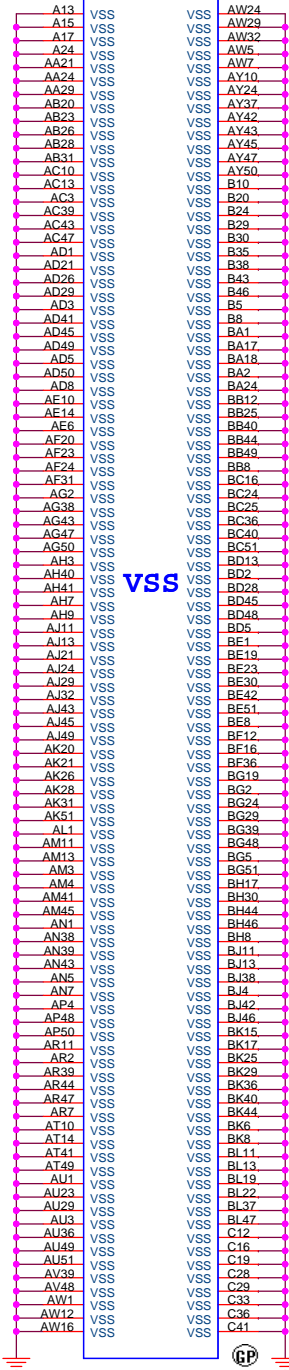
Sheet 10 of 57



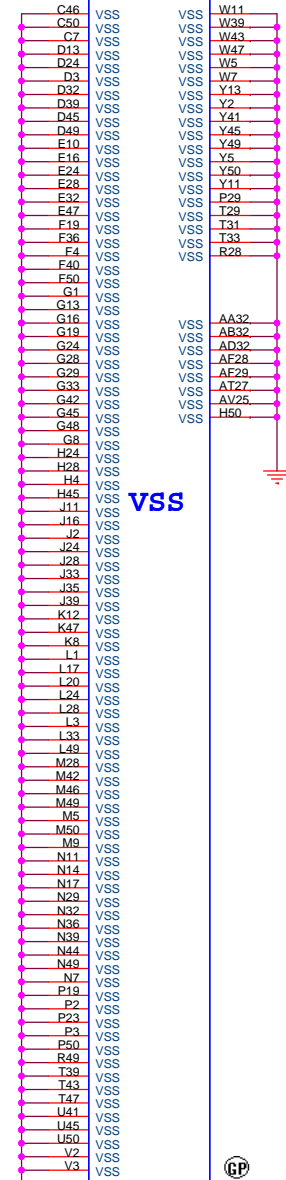
Supply	Signal Group	Icc-max
+1.05V_VCCP	VCC	1.31A
+1.05V_VCCP	VCC_NCTF	A
+1.05V_VCCP	VTT	0.85A
+1.05V_VCCP	VCC_PEG	1.2A
+1.05V_VCCP	VCC_RXR_DMI	0.25A
+1.05V_VCCP	VCC_ATX	84.15mA
+1.8V_SUS	VCC_SM	2.4A
+1.8V_SUS	VCC_SM_CK	0.2A
+1.25V_RUN	VCCA_HPLL	0.05A
+1.25V_RUN	VCCA_MPLL	0.15A
+1.25V_RUN	VCCA_SM	0.735A
+1.25V_RUN	VCCA_SM_NCTF	A
+1.25V_RUN	VCCA_SM_CK	0.015A
+1.25V_RUN	VCCD_HPLL	0.25A
+1.25V_RUN	VCCA_AXD	0.2A
+1.25V_RUN	VCCA_AXD_NCTF	A
+1.25V_RUN	VCCA_PEG_PLL	0.1A
+1.25V_RUN	VCCA_AXF	0.35A
+1.25V_RUN	VCCA_DMI	0.1A
+1.5V_RUN	VCCD_TVDAC	0.06A
+3.3V_RUN	VCCA_PEG_BG	0.005A
+3.3V_RUN	VCC_HV	0.1A



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U57J10 OF 10

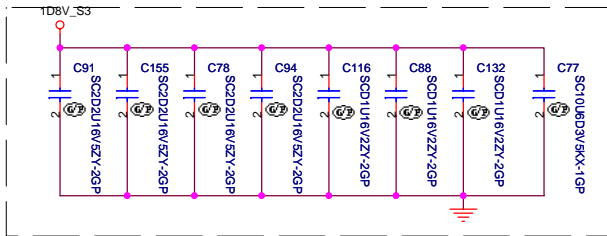


<Core Design>

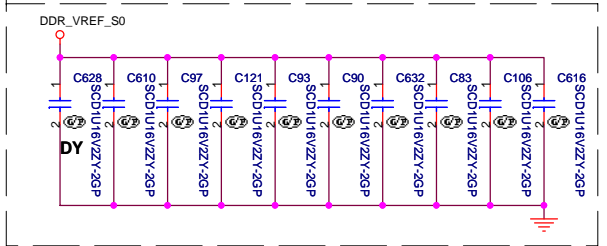
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRESTLINE(6/6)-PWR/GND		
Size	Document Number	Rev
A3	Hawke-Intel	-1
Date: Sunday, September 09, 2007		
Sheet 13 of 57		

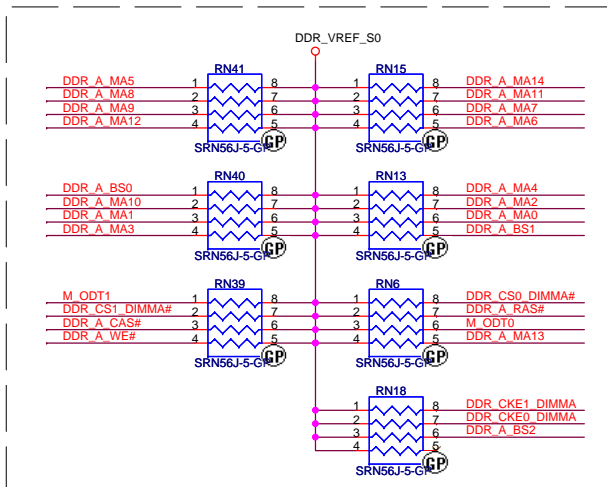
Layout Note:
Place near DM1



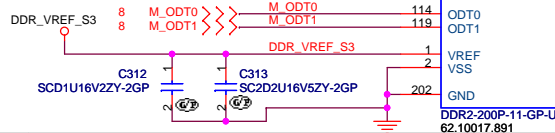
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



change to 8P4R

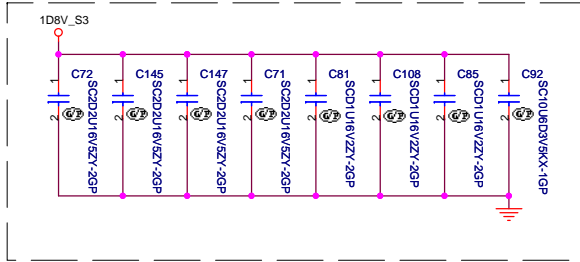


Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"

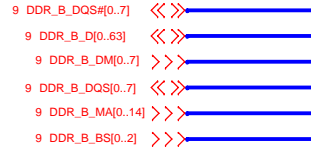
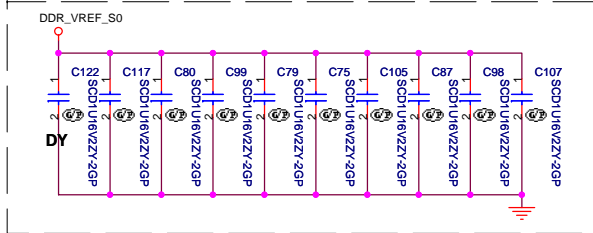


DDR A MA0	102	A0	/RAS	108	DDR A RAS#	<<<>>>	DDR A_RAS# 9
DDR A MA1	101	A1	/WE	109	DDR A WE#	<<<>>>	DDR A_WE# 9
DDR A MA2	100	A2	/CAS	113	DDR A CAS#	<<<>>>	DDR A_CAS# 9
DDR A MA3	99	A3					
DDR A MA4	98	A4					
DDR A MA5	97	A5					
DDR A MA6	96	A6					
DDR A MA7	95	A7					
DDR A MA8	94	A8					
DDR A MA9	93	A9					
DDR A MA10	92	A10/AP					
DDR A MA11	91	A11					
DDR A MA12	90	A12					
DDR A MA13	116	A13					
DDR A MA14	86	A14					
DDR A BS2	85	A15					
DDR A BS1	107	BA0					
DDR A BS1	106	BA1					
DDR A D0	5	DO0					
DDR A D1	7	DO1					
DDR A D2	17	DO2					
DDR A D3	19	DO3					
DDR A D4	4	DO4					
DDR A D5	6	DO5					
DDR A D6	16	DO6					
DDR A D7	23	DO7					
DDR A D8	24	DO8					
DDR A D9	35	DO9					
DDR A D10	25	DO10					
DDR A D11	37	DO11					
DDR A D12	20	DO12					
DDR A D13	22	DO13					
DDR A D14	38	DO14					
DDR A D15	38	DO15					
DDR A D16	43	DO16					
DDR A D17	45	DO17					
DDR A D18	56	DO18					
DDR A D19	44	DO19					
DDR A D20	46	DO20					
DDR A D21	56	DO21					
DDR A D22	58	DO22					
DDR A D23	61	DO23					
DDR A D24	63	DO24					
DDR A D25	73	DO25					
DDR A D26	75	DO26					
DDR A D27	62	DO27					
DDR A D28	64	DO28					
DDR A D29	74	DO29					
DDR A D30	76	DO30					
DDR A D31	123	DO31					
DDR A D32	125	DO32					
DDR A D33	135	DO33					
DDR A D34	137	DO34					
DDR A D35	124	DO35					
DDR A D36	126	DO36					
DDR A D37	134	DO37					
DDR A D38	136	DO38					
DDR A D39	141	DO39					
DDR A D40	143	DO40					
DDR A D41	151	DO41					
DDR A D42	153	DO42					
DDR A D43	140	DO43					
DDR A D44	142	DO44					
DDR A D45	152	DO45					
DDR A D46	154	DO46					
DDR A D47	157	DO47					
DDR A D48	159	DO48					
DDR A D49	173	DO49					
DDR A D50	175	DO50					
DDR A D51	168	DO51					
DDR A D52	160	DO52					
DDR A D53	174	DO53					
DDR A D54	176	DO54					
DDR A D55	179	DO55					
DDR A D56	181	DO56					
DDR A D57	189	DO57					
DDR A D58	191	DO58					
DDR A D59	180	DO59					
DDR A D60	182	DO60					
DDR A D61	192	DO61					
DDR A D62	189	DO62					
DDR A D63	194	DO63					
DDR A DQS#0	11	/DO50					
DDR A DQS#1	23	/DO51					
DDR A DQS#2	49	/DO52					
DDR A DQS#3	68	/DO53					
DDR A DQS#4	129	/DO54					
DDR A DQS#5	146	/DO55					
DDR A DQS#6	167	/DO56					
DDR A DQS#7	186	/DO57					
DDR A DQS0	13	DO50					
DDR A DQS1	31	DO51					
DDR A DQS2	51	DO52					
DDR A DQS3	70	DO53					
DDR A DQS4	131	DO54					
DDR A DQS5	148	DO55					
DDR A DQS6	169	DO56					
DDR A DQS7	188	DO57					
DDR A DQS0	11	DO58					
DDR A DQS1	23	DO59					
DDR A DQS2	49	DO60					
DDR A DQS3	68	DO61					
DDR A DQS4	129	DO62					
DDR A DQS5	146	DO63					
DDR A DQS6	167	DO64					
DDR A DQS7	186	DO65					
DDR A DQS0	13	DO66					
DDR A DQS1	31	DO67					
DDR A DQS2	51	DO68					
DDR A DQS3	70	DO69					
DDR A DQS4	131	DO70					
DDR A DQS5	148	DO71					
DDR A DQS6	169	DO72					
DDR A DQS7	188	DO73					
DDR A DQS0	11	DO74					
DDR A DQS1	23	DO75					
DDR A DQS2	49	DO76					
DDR A DQS3	68	DO77					
DDR A DQS4	129	DO78					
DDR A DQS5	146	DO79					
DDR A DQS6	167	DO80					
DDR A DQS7	186	DO81					
DDR A DQS0	13	DO82					
DDR A DQS1	31	DO83					
DDR A DQS2	51	DO84					
DDR A DQS3	70	DO85					
DDR A DQS4	131	DO86					
DDR A DQS5	148	DO87					
DDR A DQS6	169	DO88					
DDR A DQS7	188	DO89					
DDR A DQS0	11	DO90					
DDR A DQS1	23	DO91					
DDR A DQS2	49	DO92					
DDR A DQS3	68	DO93					
DDR A DQS4	129	DO94					
DDR A DQS5	146	DO95					
DDR A DQS6	167	DO96					
DDR A DQS7	186	DO97					
DDR A DQS0	13	DO98					
DDR A DQS1	31	DO99					
DDR A DQS2	51	DO100					
DDR A DQS3	70	DO101					
DDR A DQS4	131	DO102					
DDR A DQS5	148	DO103					
DDR A DQS6	169	DO104					
DDR A DQS7	188	DO105					
DDR A DQS0	11	DO106					
DDR A DQS1	23	DO107					
DDR A DQS2	49	DO108					
DDR A DQS3	68	DO109					
DDR A DQS4	129	DO110					
DDR A DQS5	146	DO111					
DDR A DQS6	167	DO112					
DDR A DQS7	186	DO113					
DDR A DQS0	13	DO114					
DDR A DQS1	31	DO115					
DDR A DQS2	51	DO116					
DDR A DQS3	70	DO117					
DDR A DQS4	131	DO118					
DDR A DQS5	148	DO119					
DDR A DQS6	169	DO120					
DDR A DQS7	188	DO121					
DDR A DQS0	11	DO122					
DDR A DQS1	23	DO123					
DDR A DQS2	49	DO124					
DDR A DQS3	68	DO125					
DDR A DQS4	129	DO126					
DDR A DQS5	146	DO127					
DDR A DQS6	167	DO128					
DDR A DQS7	186	DO129					
DDR A DQS0	13	DO130					
DDR A DQS1	31	DO131					
DDR A DQS2	51	DO132					
DDR A DQS3	70	DO133					
DDR A DQS4	131	DO134					
DDR A DQS5	148	DO135					
DDR A DQS6	169	DO136					
DDR A DQS7	188	DO137					
DDR A DQS0	11	DO138					
DDR A DQS1	23	DO139					
DDR A DQS2	49	DO140					
DDR A DQS3	68	DO141					
DDR A DQS4	129	DO142					
DDR A DQS5	146	DO143					
DDR A DQS6	167	DO144					
DDR A DQS7	186	DO145					
DDR A DQS0	13	DO146					
DDR A DQS1	31	DO147					
DDR A DQS2	51	DO148					
DDR A DQS3	70	DO149					
DDR A DQS4	131	DO150					
DDR A DQS5	148	DO151					
DDR A DQS6	169	DO152					
DDR A DQS7	188	DO153					
DDR A DQS0	11	DO154					
DDR A DQS1	23	DO155					
DDR A DQS2	49	DO156					
DDR A DQS3	68	DO157					
DDR A DQS4	129	DO158					
DDR A DQS5	146	DO159					
DDR A DQS6	167	DO160					
DDR A DQS7	186	DO161					
DDR A DQS0	13	DO162					
DDR A DQS1	31	DO163					
DDR A DQS2	51	DO164					
DDR A DQS3	70	DO165					
DDR A DQS4	131	DO166					
DDR A DQS5	148	DO167					
DDR A DQS6	169	DO168					
DDR A DQS7	188	DO169					
DDR A DQS0	11	DO170					
DDR A DQS1	23	DO171					
DDR A DQS2	49	DO172					
DDR A DQS3	68	DO173					
DDR A DQS4	129	DO174					
DDR A DQS5	146	DO175					
DDR A DQS6	167	DO176					
DDR A DQS7	186	DO177					
DDR A DQS0	13	DO178					
DDR A DQS1	31	DO179					
DDR A DQS2	51	DO180					
DDR A DQS3	70	DO181					
DDR A DQS4	131	DO182					
DDR A DQS5	148	DO183					
DDR A DQS6	169	DO184					
DDR A DQS7	188	DO185					
DDR A DQS0	11	DO186					
DDR A DQS1	23	DO187					
DDR A DQS2	49	DO188					
DDR A DQS3	68	DO189					
DDR A DQS4	129	DO190					
DDR A DQS5	146	DO191					
DDR A DQS6	167	DO192					
DDR A DQS7	186	DO193					
DDR A DQS0	13	DO194					
DDR A DQS1	31	DO195					
DDR A DQS2	51	DO196					
DDR A DQS3	70	DO197					
DDR A DQS4	131	DO198					
DDR A DQS5	148	DO199					
DDR A DQS6	169	DO200					
DDR A DQS7	188	DO201					
DDR A DQS0	11	DO202					
DDR A DQS1	23	DO203					
DDR A DQS2	49	DO204					
DDR A DQS3	68	DO205					
DDR A DQS4	129	DO206					
DDR A DQS5	1						

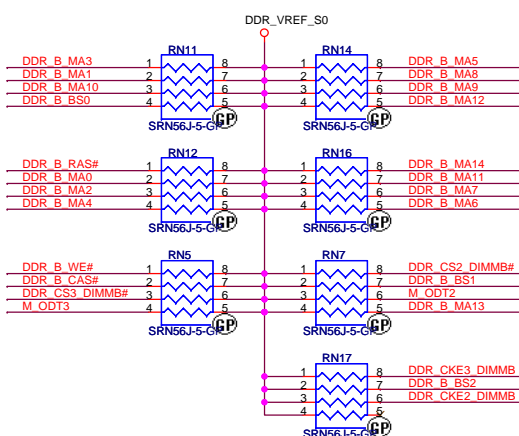
Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



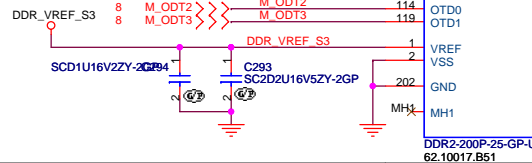
Layout Note:
Place these resistors closely DM2,all trace length Max=1.5"



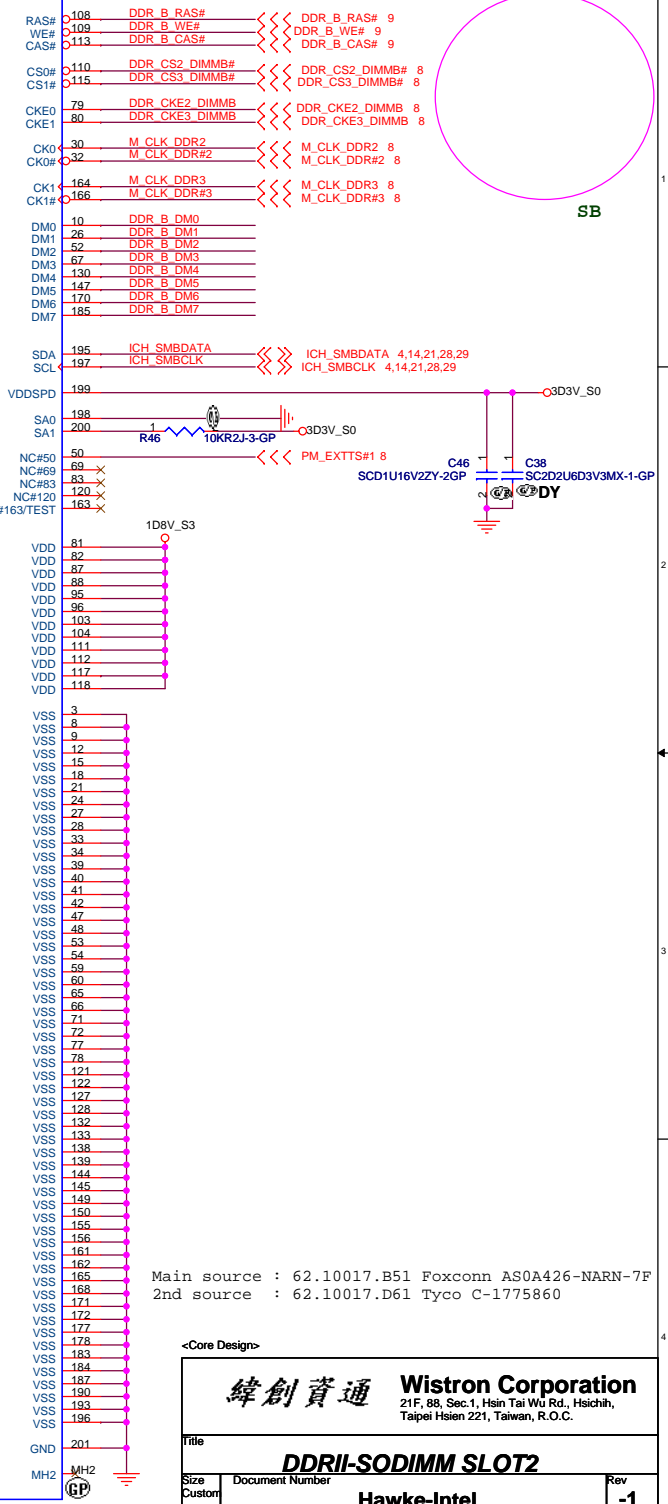
DDR_B_MA0	102
DDR_B_MA1	101
DDR_B_MA2	100
DDR_B_MA3	99
DDR_B_MA4	98
DDR_B_MA5	97
DDR_B_MA6	96
DDR_B_MA7	95
DDR_B_MA8	94
DDR_B_MA9	93
DDR_B_MA10	92
DDR_B_MA11	91
DDR_B_MA12	90
DDR_B_MA13	89
DDR_B_MA14	88
DDR_B_BS2	84
DDR_B_BS1	85

DDR_B_D0	5
DDR_B_D1	7
DDR_B_D2	17
DDR_B_D3	19
DDR_B_D4	1
DDR_B_D5	6
DDR_B_D6	14
DDR_B_D7	16
DDR_B_D8	23
DDR_B_D9	25
DDR_B_D10	35
DDR_B_D11	37
DDR_B_D12	20
DDR_B_D13	22
DDR_B_D14	36
DDR_B_D15	38
DDR_B_D16	43
DDR_B_D17	45
DDR_B_D18	55
DDR_B_D19	44
DDR_B_D20	57
DDR_B_D21	46
DDR_B_D22	56
DDR_B_D23	58
DDR_B_D24	61
DDR_B_D25	63
DDR_B_D26	73
DDR_B_D27	75
DDR_B_D28	62
DDR_B_D29	64
DDR_B_D30	74
DDR_B_D31	76
DDR_B_D32	123
DDR_B_D33	125
DDR_B_D34	135
DDR_B_D35	137
DDR_B_D36	124
DDR_B_D37	126
DDR_B_D38	134
DDR_B_D39	136
DDR_B_D40	141
DDR_B_D41	143
DDR_B_D42	151
DDR_B_D43	153
DDR_B_D44	140
DDR_B_D45	142
DDR_B_D46	152
DDR_B_D47	154
DDR_B_D48	157
DDR_B_D49	159
DDR_B_D50	173
DDR_B_D51	175
DDR_B_D52	158
DDR_B_D53	160
DDR_B_D54	174
DDR_B_D55	176
DDR_B_D56	179
DDR_B_D57	181
DDR_B_D58	189
DDR_B_D59	191
DDR_B_D60	180
DDR_B_D61	182
DDR_B_D62	192
DDR_B_D63	194

DDR_B_DQS#0	11
DDR_B_DQS#1	25
DDR_B_DQS#2	49
DDR_B_DQS#3	68
DDR_B_DQS#4	129
DDR_B_DQS#5	146
DDR_B_DQS#6	167
DDR_B_DQS#7	186
DDR_B_DQS0	13
DDR_B_DQS1	31
DDR_B_DQS2	51
DDR_B_DQS3	70
DDR_B_DQS4	131
DDR_B_DQS5	148
DDR_B_DQS6	169
DDR_B_DQS7	188



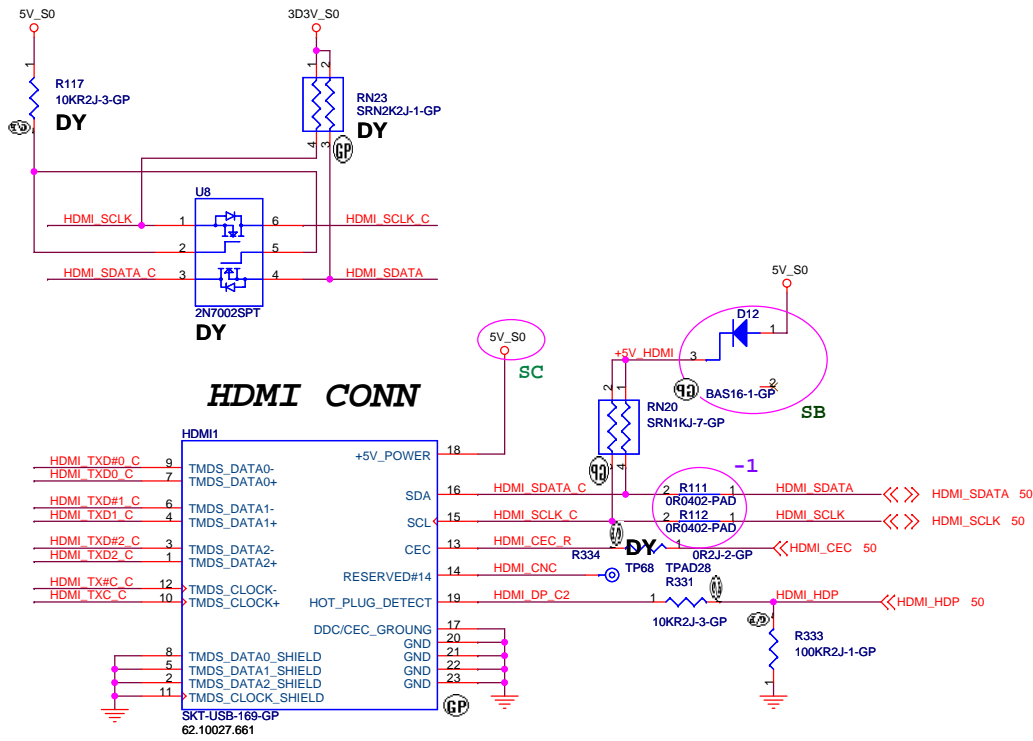
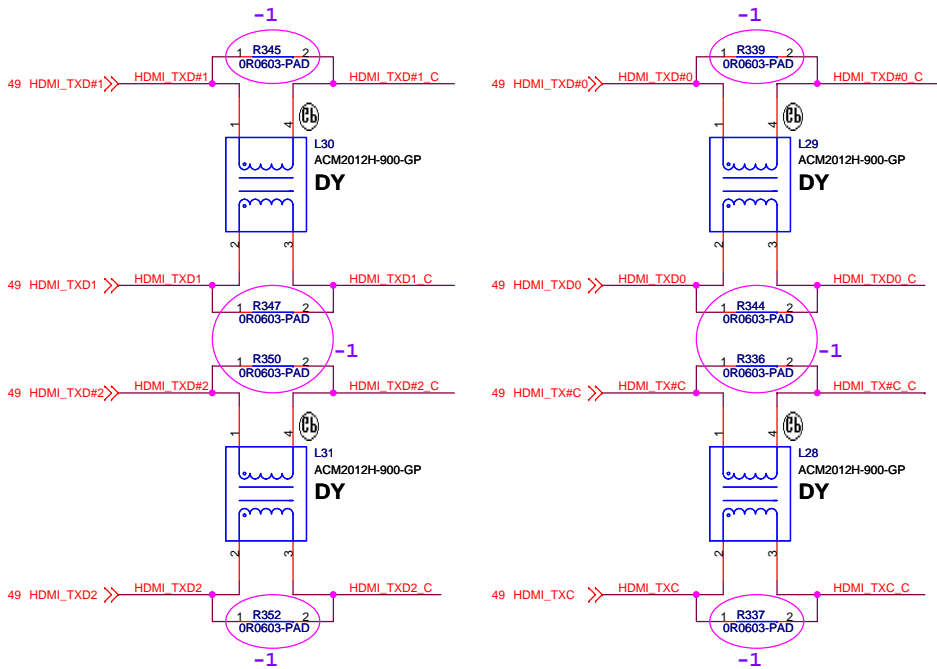
REVERSE TYPE High 9.2 mm



Main source : 62.10017.B51 Foxconn AS0A426-NARN-7F
2nd source : 62.10017.D61 Tyco C-1775860

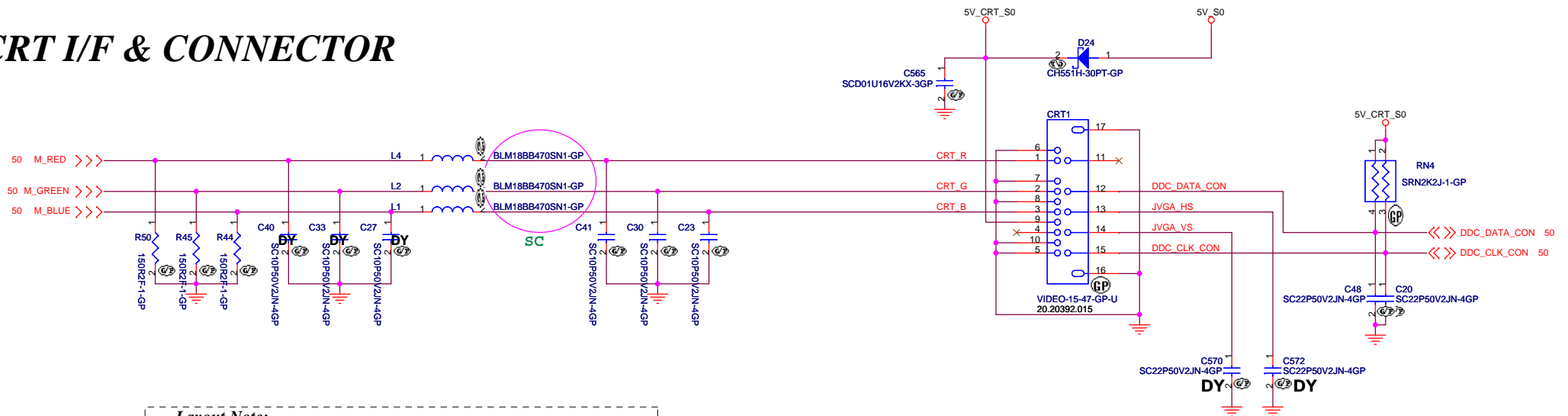
<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>DDRII-SODIMM SLOT2</p>		
<p>File</p>	<p>Document Number</p>	<p>Rev</p>
<p>Size</p>	<p>Hawke-Intel</p>	<p>-1</p>
<p>Custom</p>	<p>Date: Sunday, September 09, 2007</p>	<p>Sheet 15 of 57</p>

HDMI I/F & CONNECTOR



Main source : 62.10027.661 Molex 47408-0201
2nd source : 62.10078.121 Tyco C1759548-1

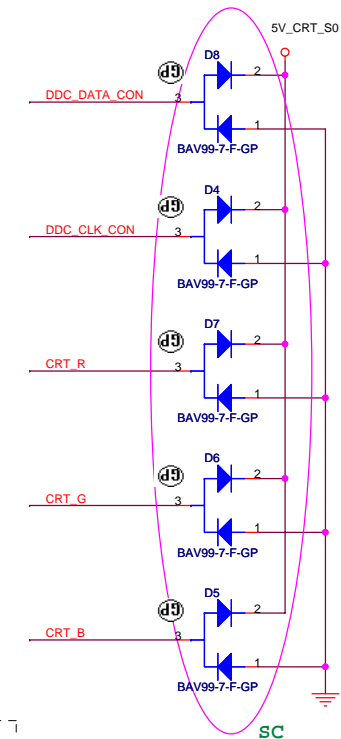
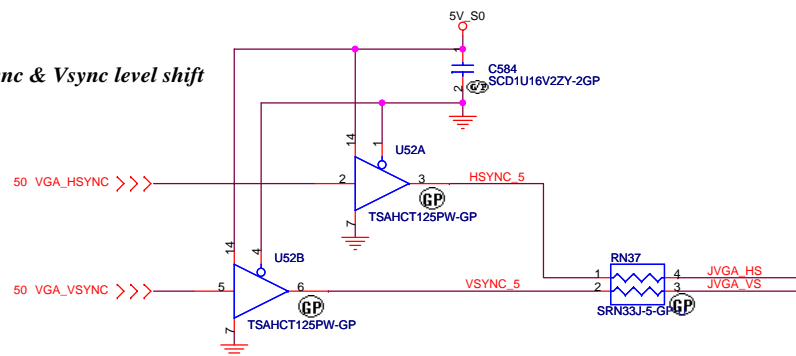
CRT I/F & CONNECTOR



Layout Note:

Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift



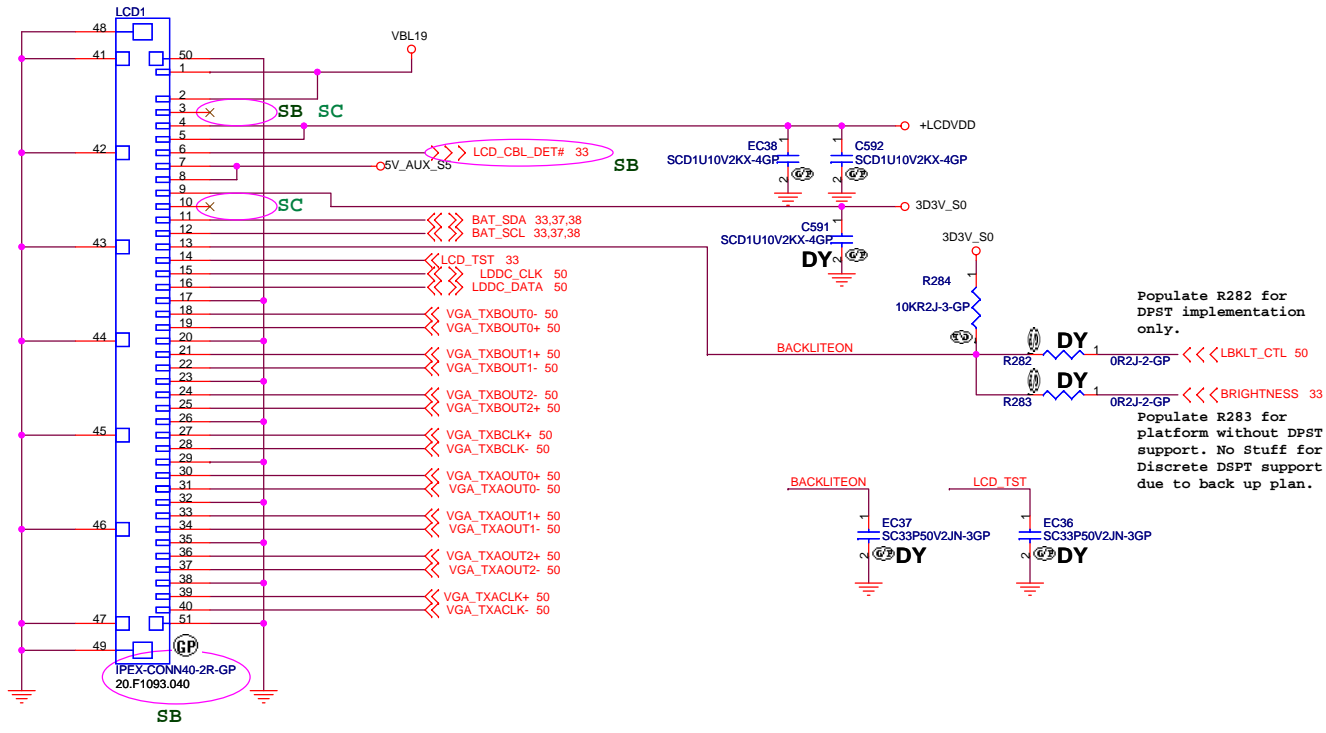
TP28-75-GP	TP177	1	5V_CRT_S0
TP28-75-GP	TP176	1	DDC_DATA_CON
TP28-75-GP	TP179	1	DDC_CLK_CON
TP28-75-GP	TP178	1	CRT_R
TP28-75-GP	TP180	1	CRT_G
TP28-75-GP	TP182	1	CRT_B
TP28-75-GP	TP181	1	Jvga_HS
TP28-75-GP	TP183	1	Jvga_VS

For AFTE, place them on the some side.

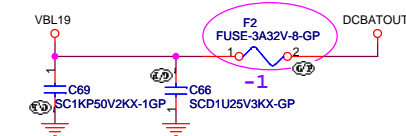
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT Connector	
Size A3	Document Number	Rev
	Hawke-Intel	-1
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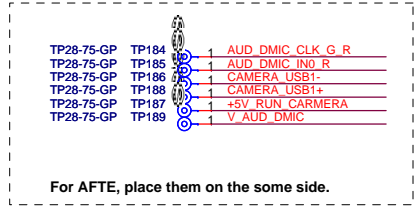
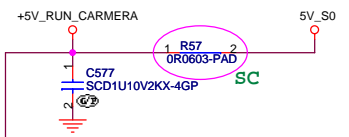
INVERTER POWER



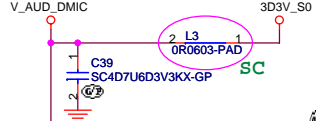
Populate R282 for DPST implementation only.

Populate R283 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.

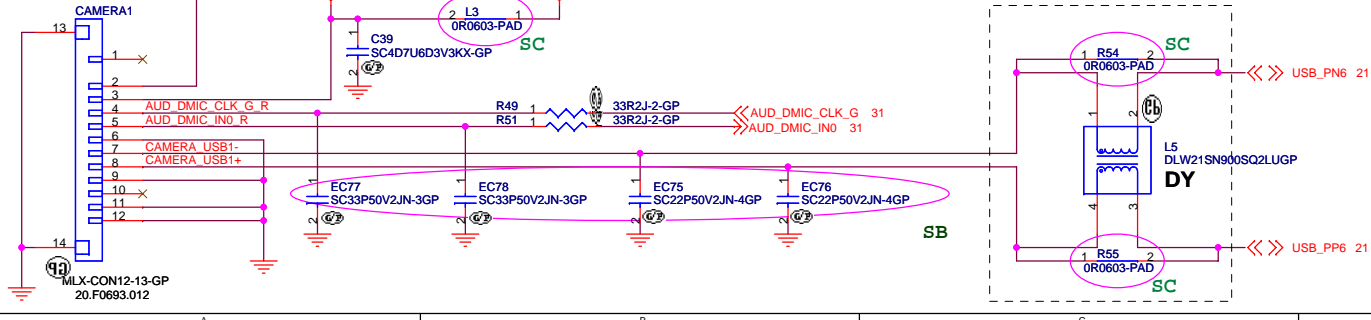
CAMERA Power



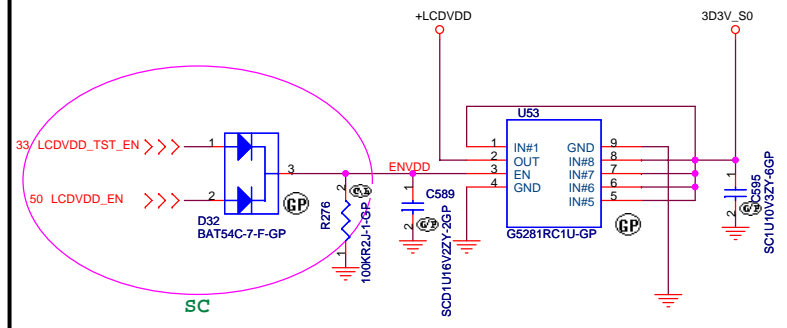
Mic Power

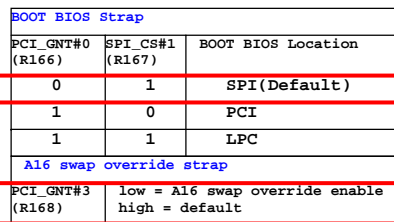
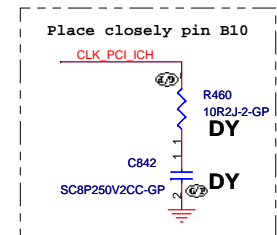


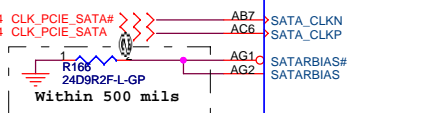
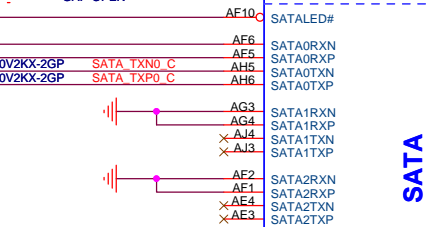
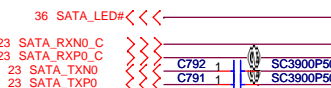
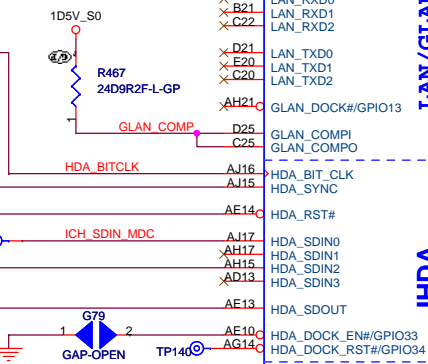
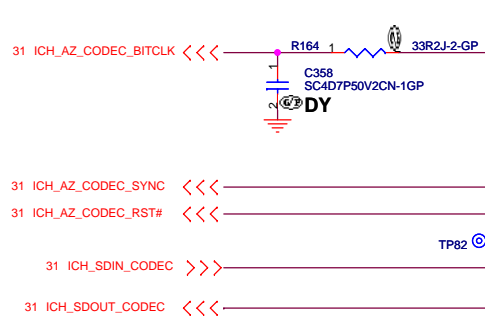
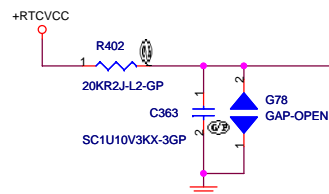
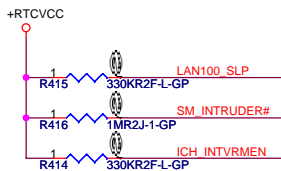
Place near connector CAMERA1.



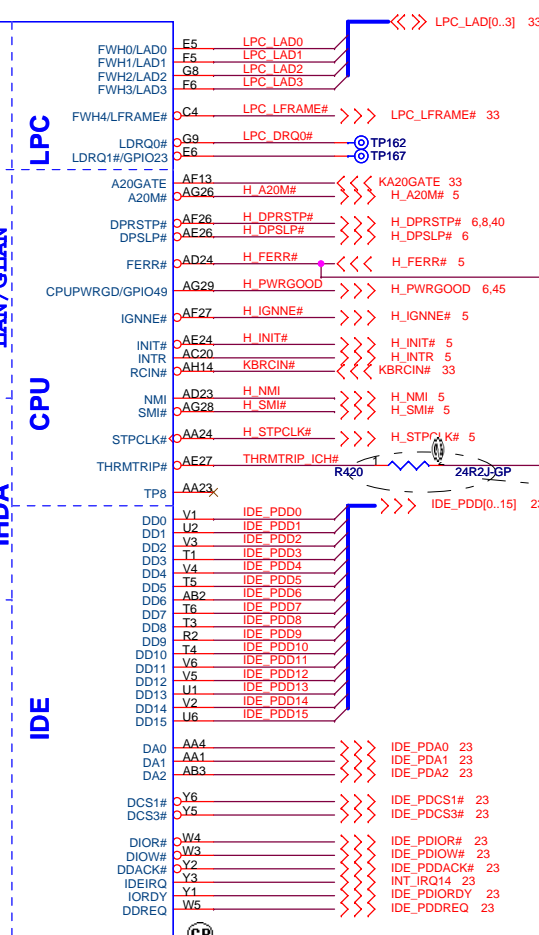
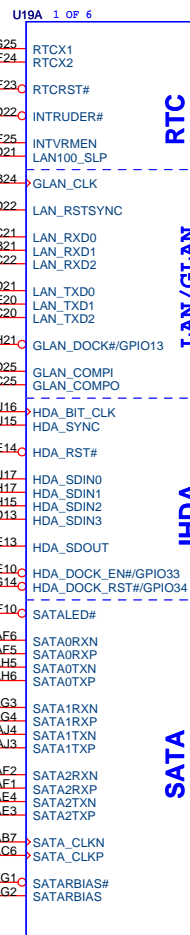
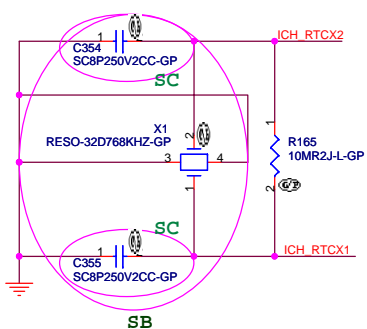
LCD POWER



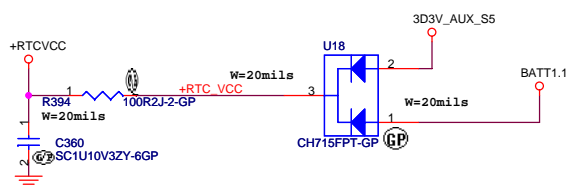




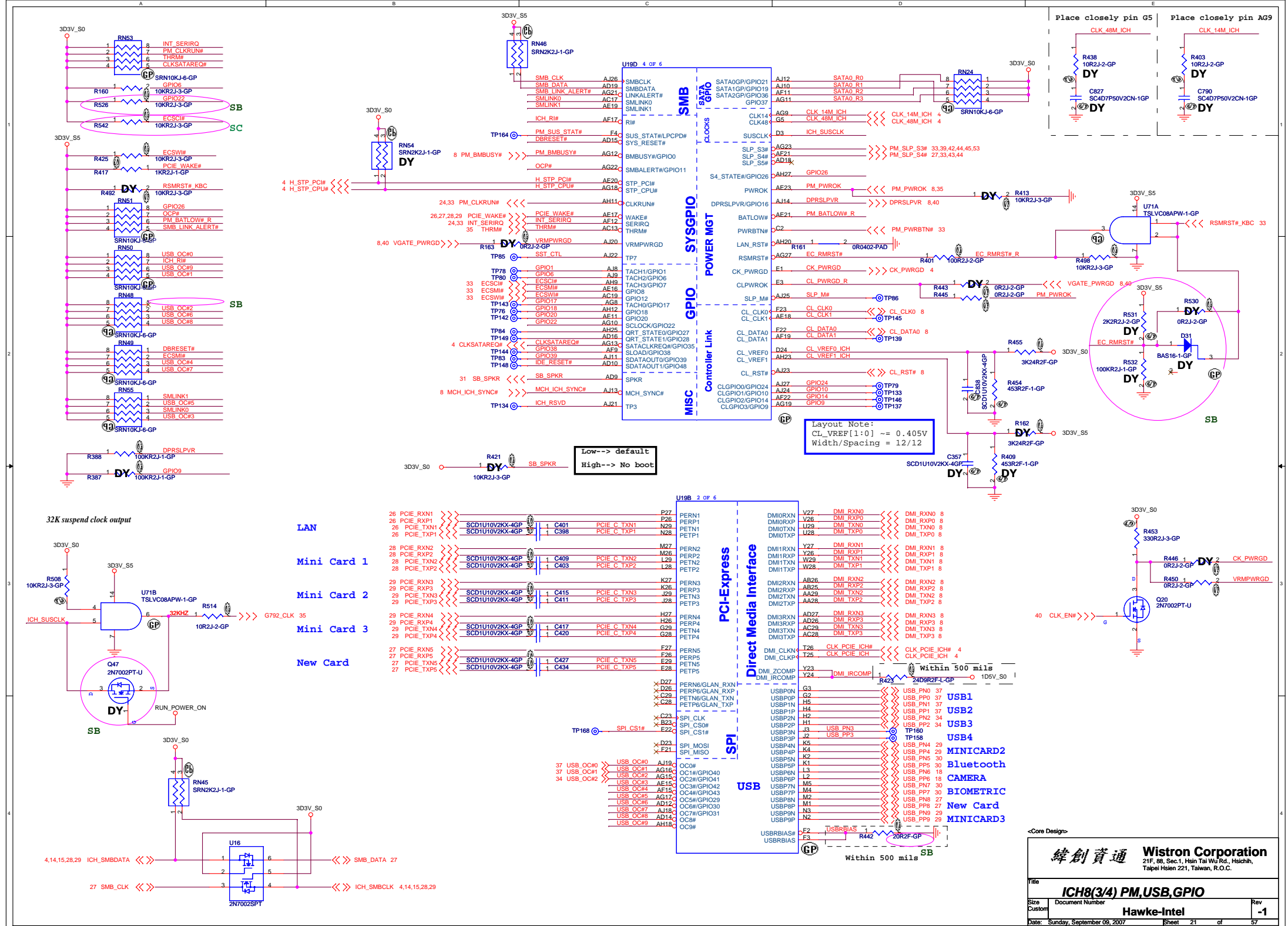
X1 CL=12.5pF±0.2pF
Freq. Tolerance:±20ppm

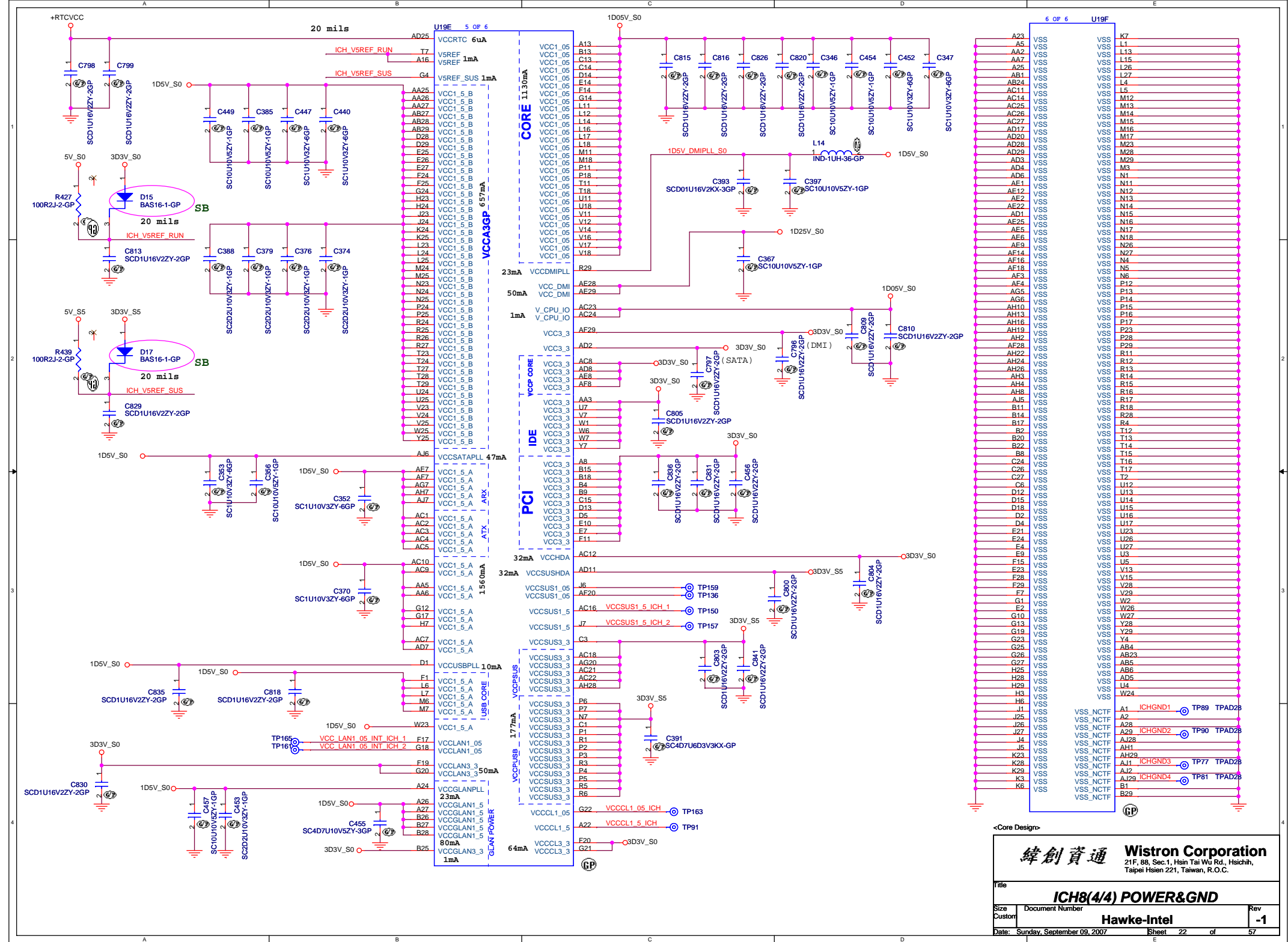


RTC POWER

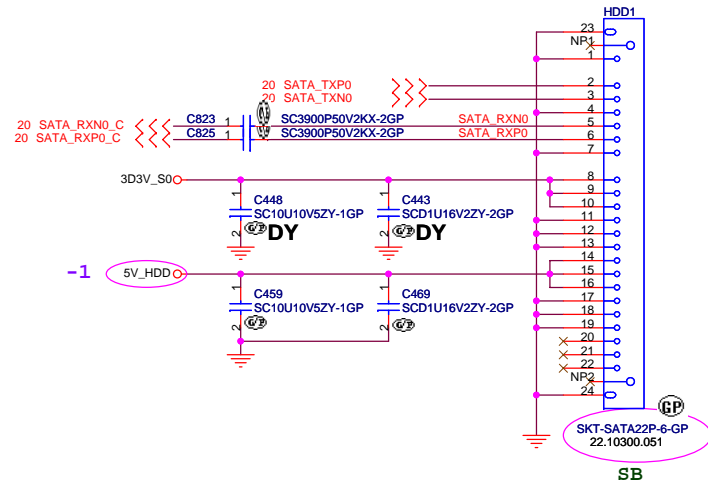


<Core Design>

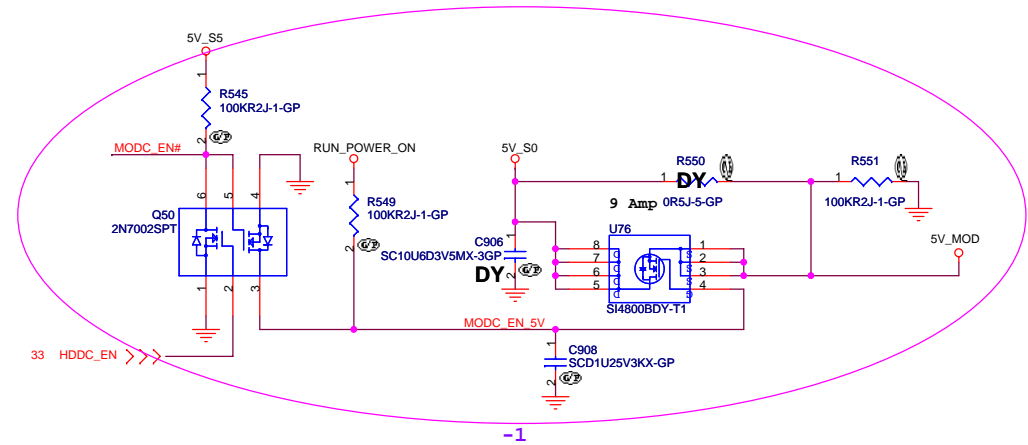
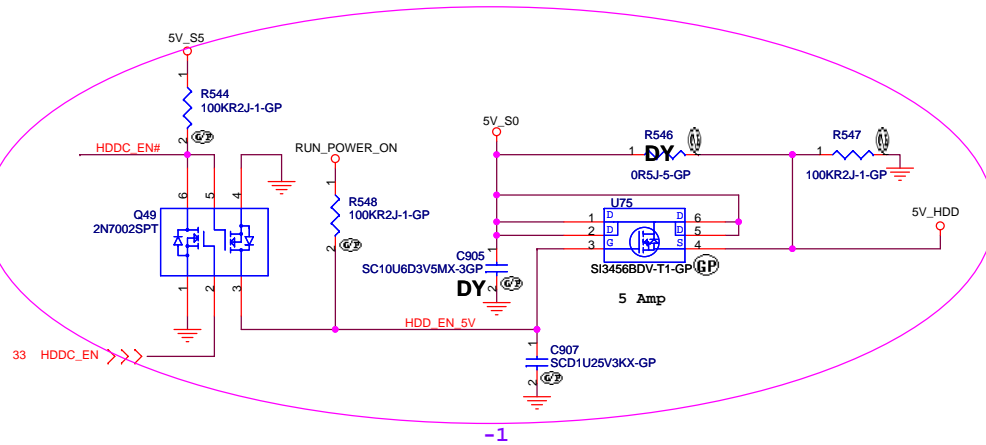
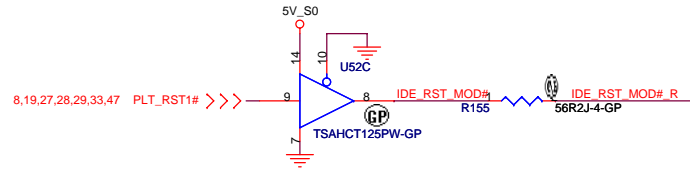
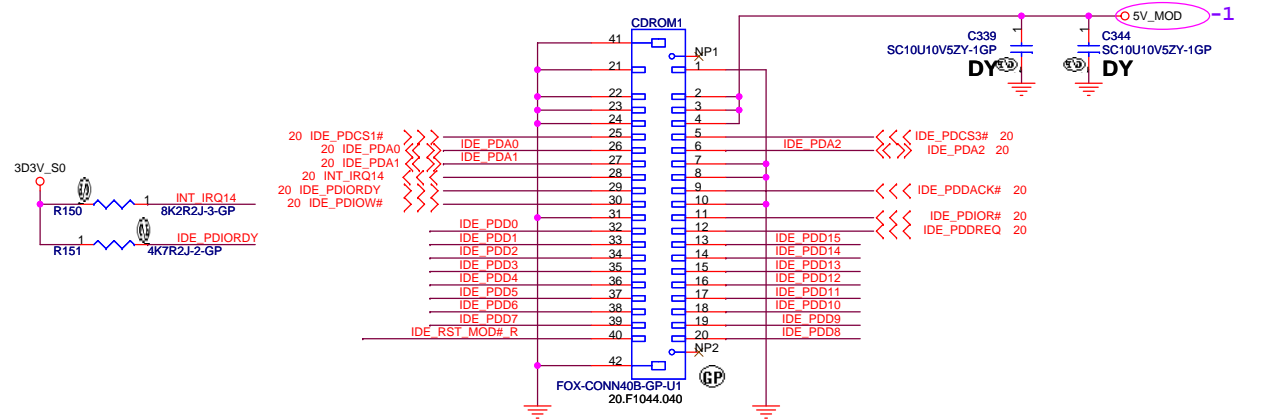




SATA HDD Connector



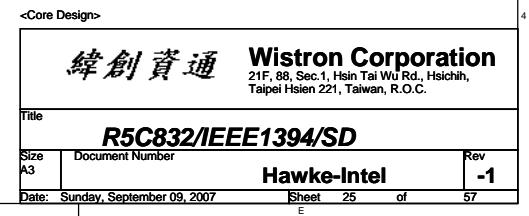
ODD Connector



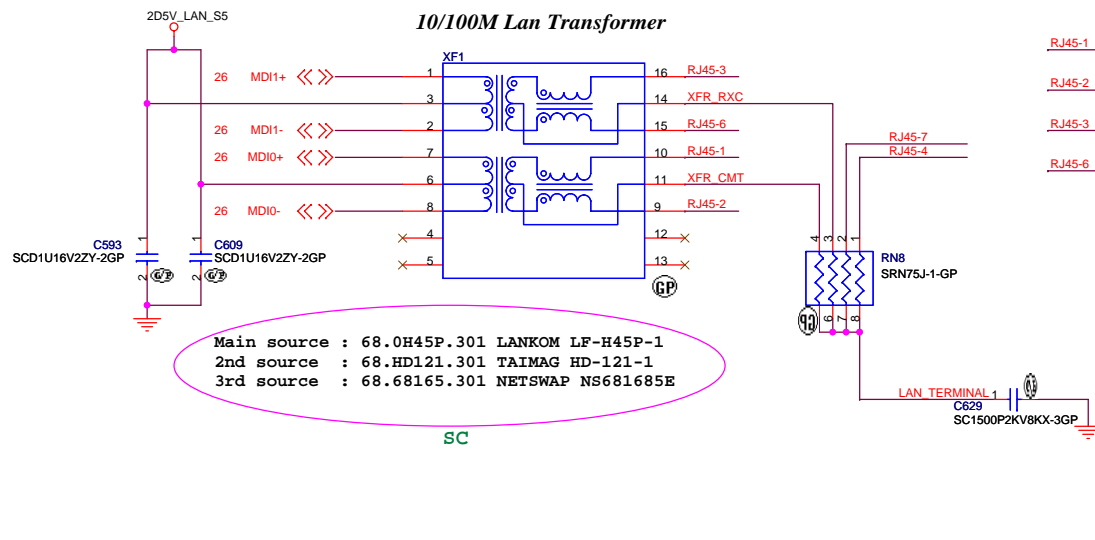
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

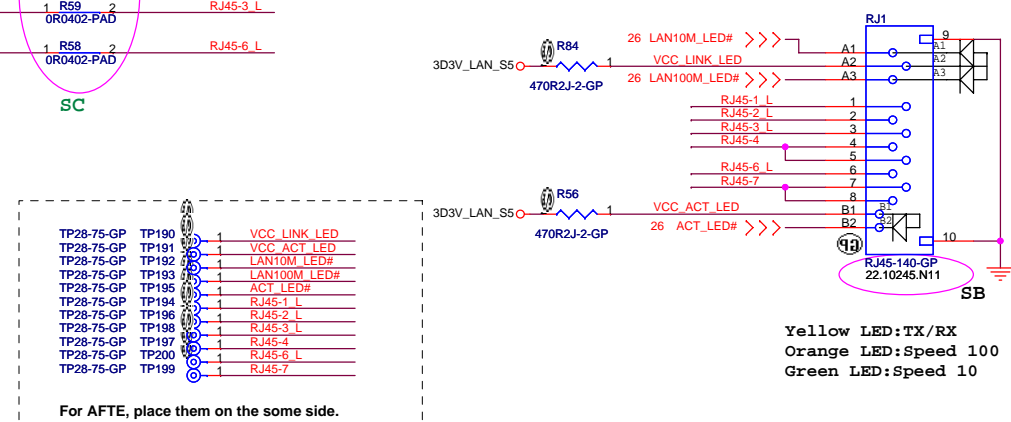
Title			HDD/ODD	
Size A3	Document Number	Hawke-Intel		Rev -1
Date: Sunday, September 09, 2007	Sheet 23	of	57	



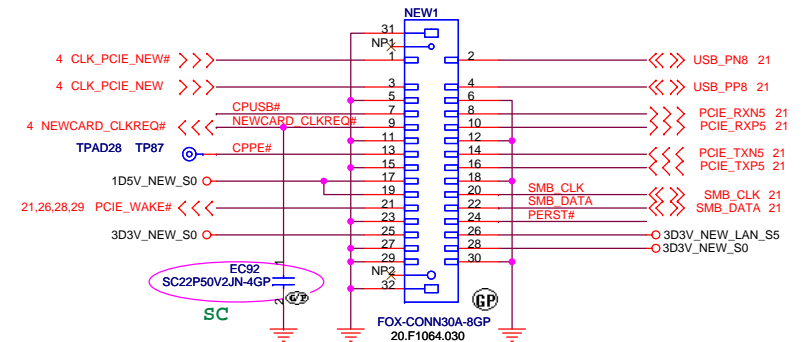
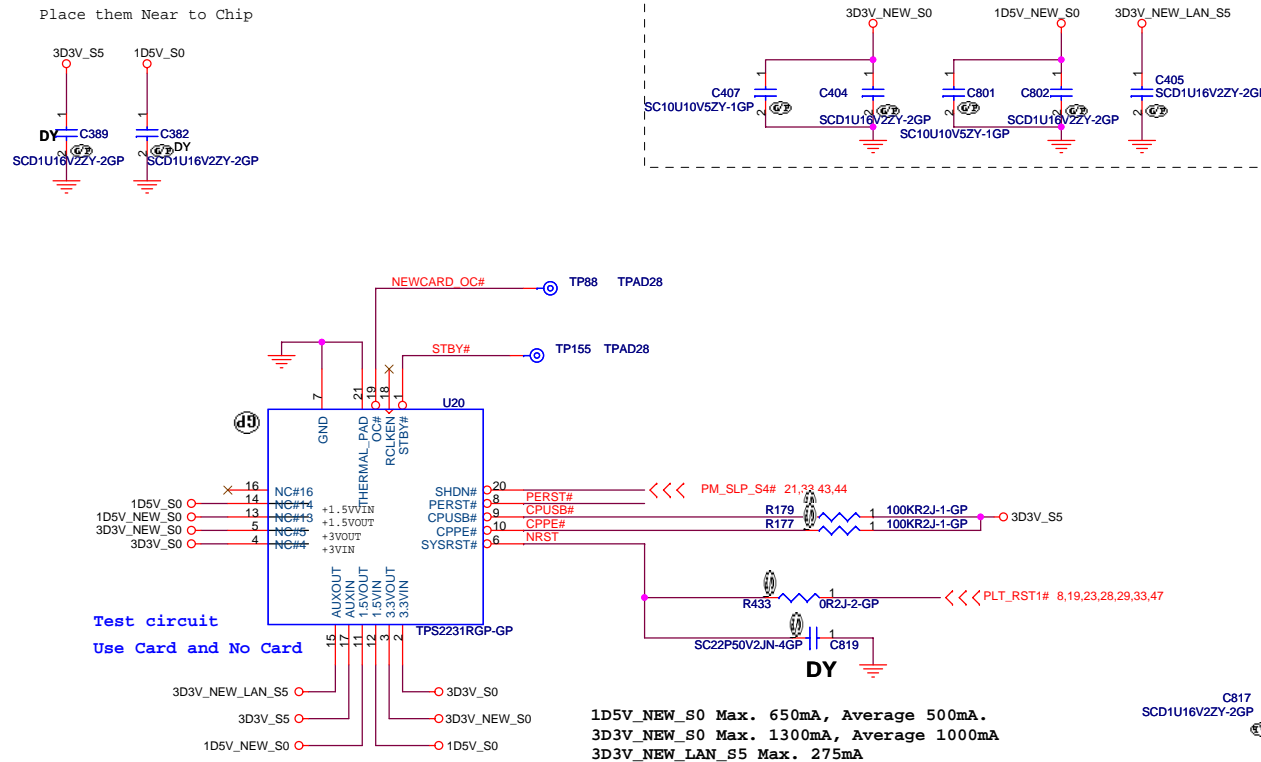
RJ45 Connector



1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



NEWCARD Connector

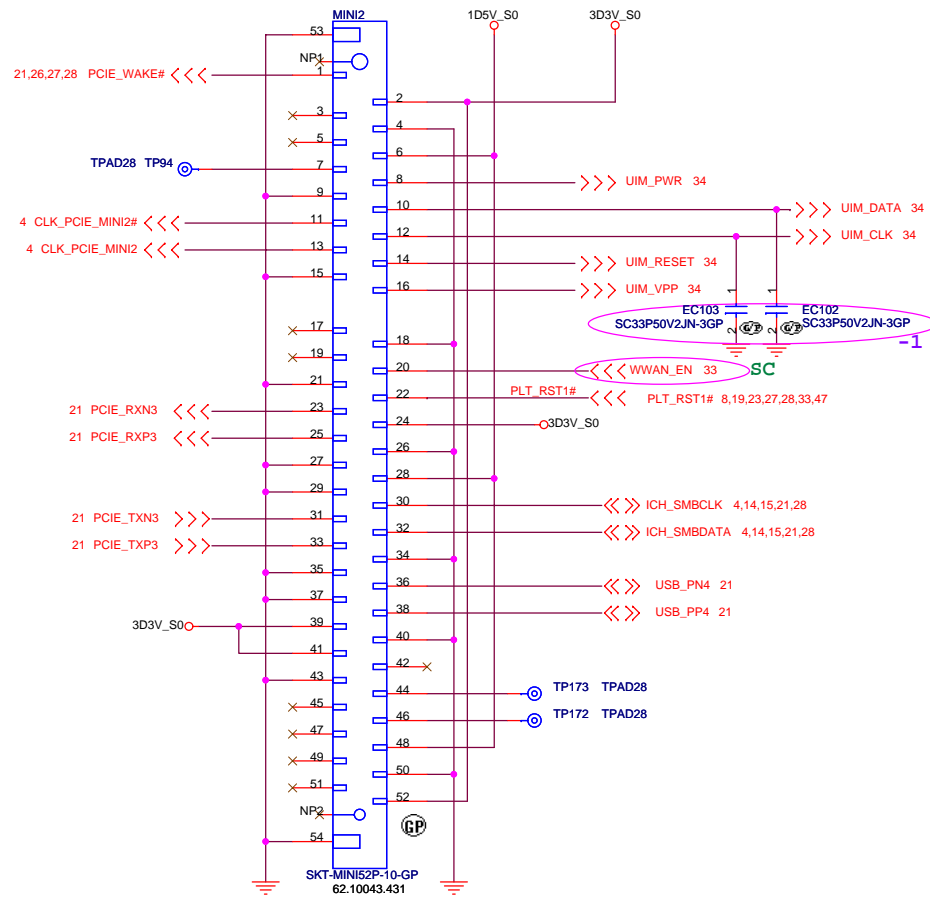


Main source : 20.F0992.052 P-Two A54452-A0G16-N
2nd source : 62.10043.551 Tyco 1759553-1

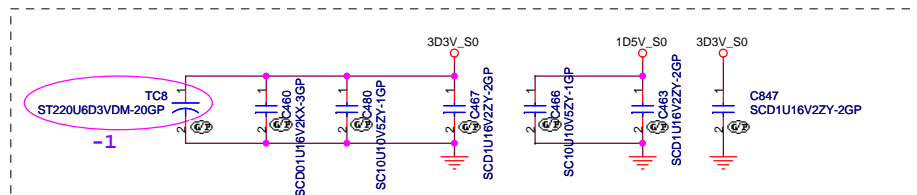


Mini Card Connector

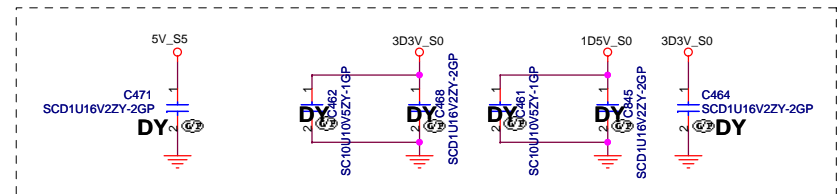
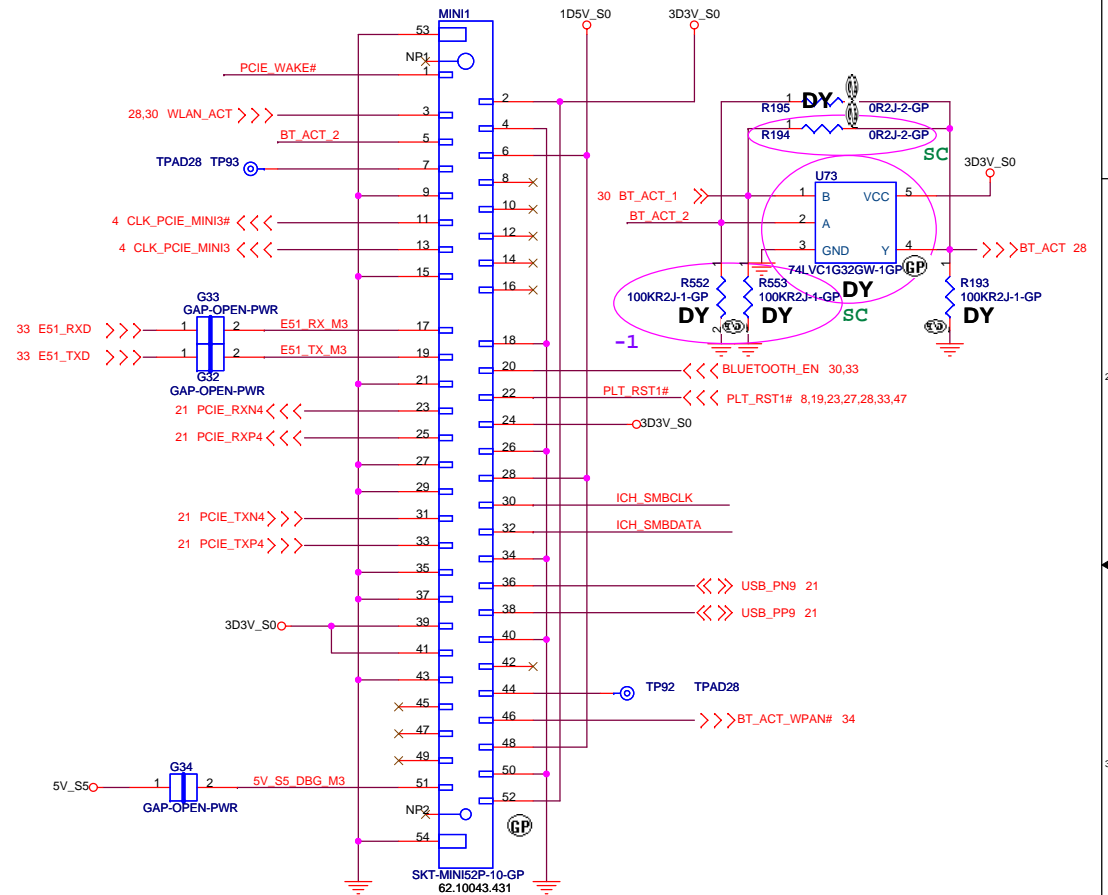
Mini Card Connector 2(WWAN)

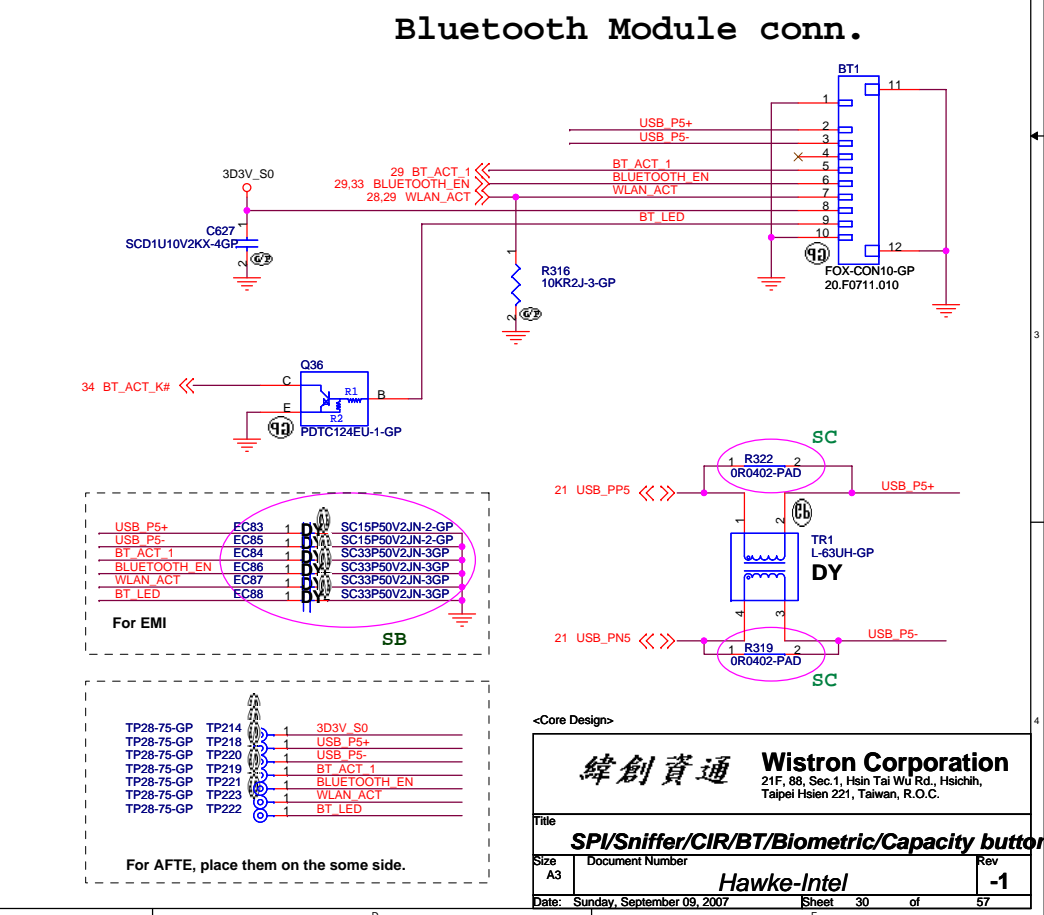
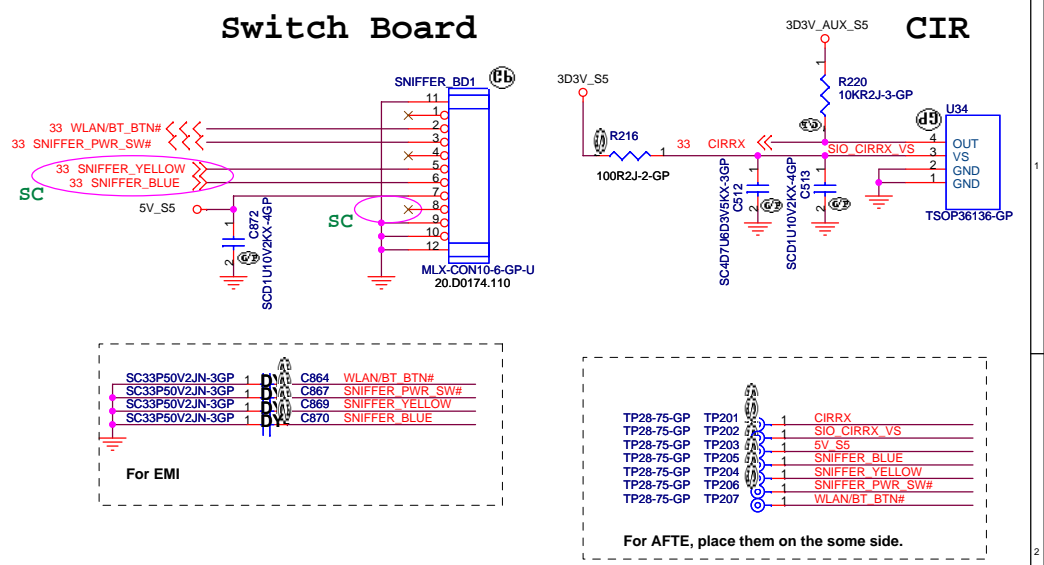
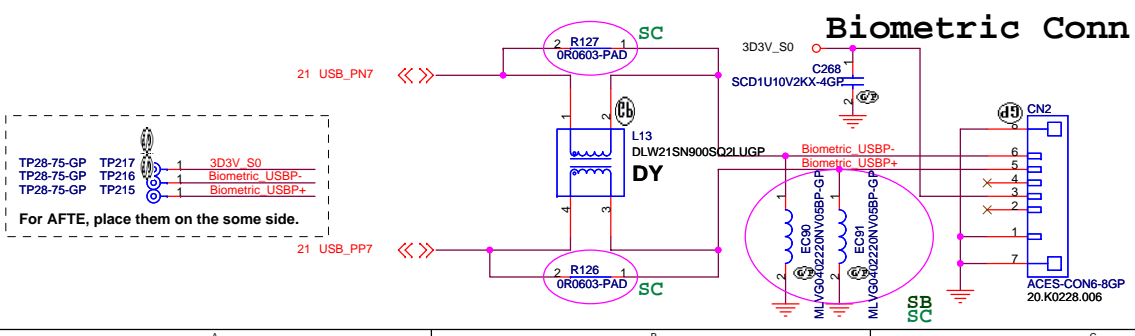
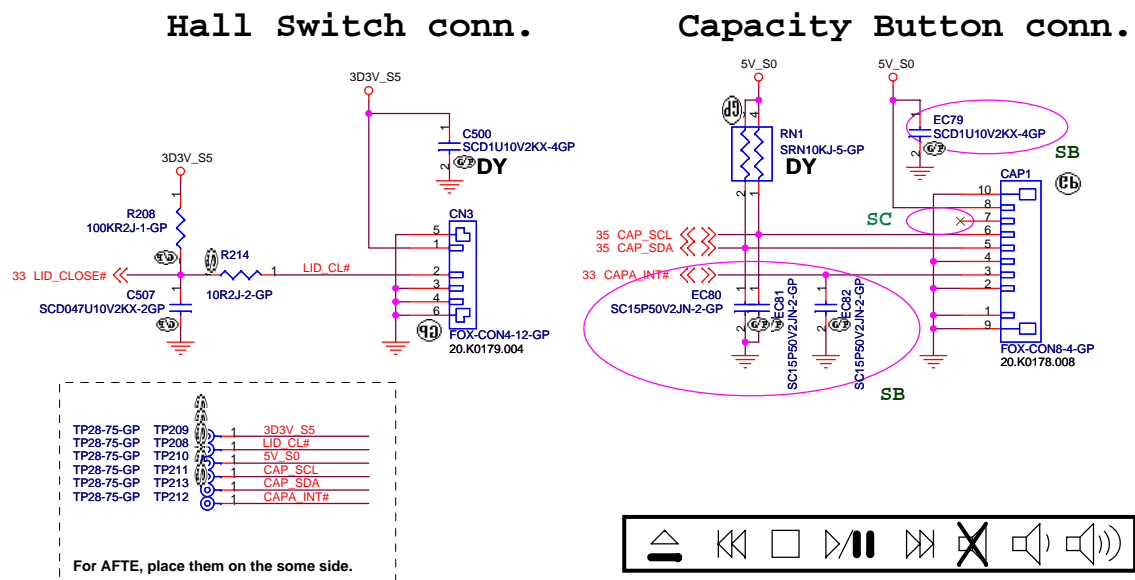
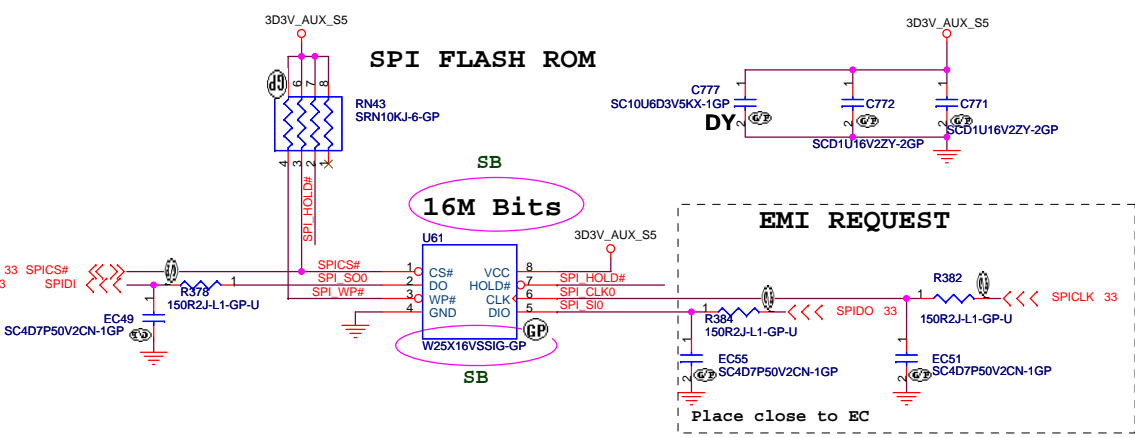


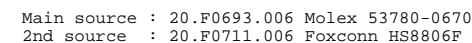
Main source : 20.F0992.052 P-Two A54452-A0G16-N
2nd source : 62.10043.551 Tyco 1759553-1



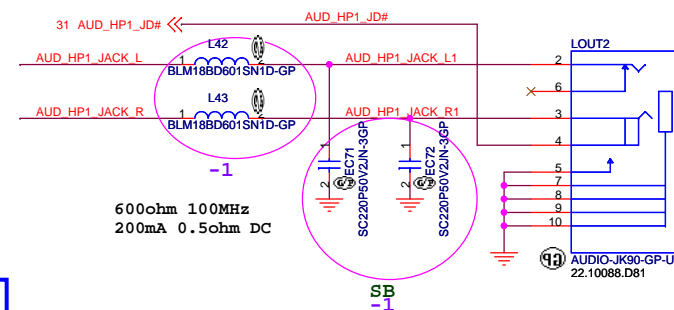
Mini Card Connector 3(Robson/BT)



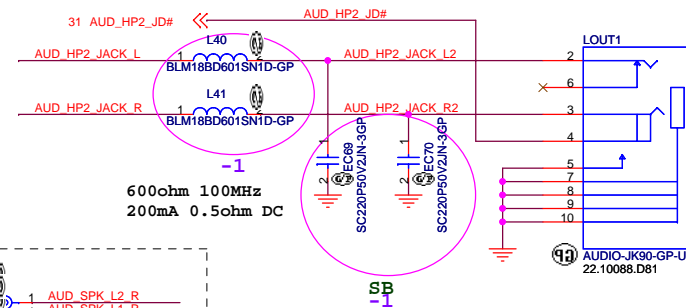




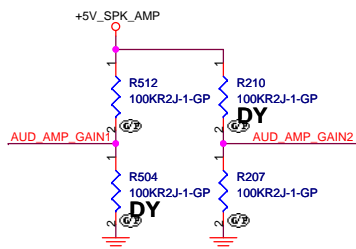
LINE1 OUT



LINE2 OUT

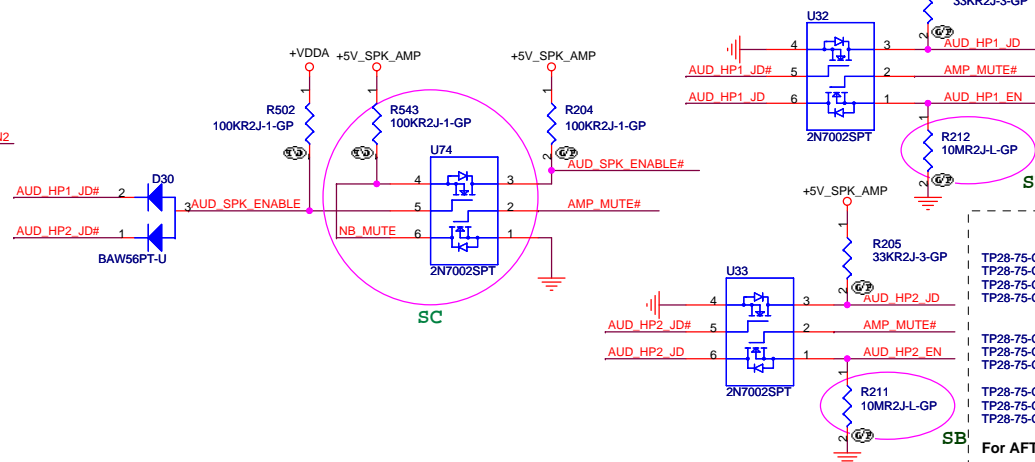


GAIN SETTING



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown



TP227-75-GP TP227 1 AUD SPK L2 R

TP228-75-GP TP228 1 AUD SPK L1 R

TP230-75-GP TP230 1 AUD SPK R2 R

TP229-75-GP TP229 1 AUD SPK R1 R

TP232-75-GP TP232 1 AUD HP1 JD#

TP231-75-GP TP231 1 AUD HP1 JACK L1

TP233-75-GP TP233 1 AUD HP1 JACK R1

TP234-75-GP TP234 1 AUD HP2 JD#

TP235-75-GP TP235 1 AUD HP2 JACK L2

TP236-75-GP TP236 1 AUD HP2 JACK R2

For AFTE, place them on the same side.

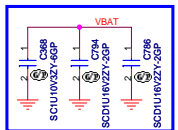
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

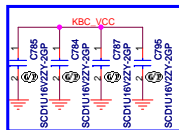
Title	AUDIO AMP/SPEAKER
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Size A3	Document Number Hawke-Intel	Rev -1
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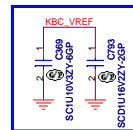
Date: Sunday, September 09, 2007 Sheet 32 of 57



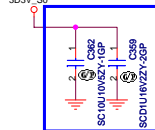
PLACE CAP NEAR PIN80 AND PIN102



PLACE CAP NEAR PIN46,19,115,76,88



PLACE CAP NEAR PIN104



PLACE CAP Close to Pin 4

WPC8763L STRAP PIN

JEN0 (Pin 24)	JENK (Pin 53)	Functionality of Pins 17, 20, 21, 23, 25, 27	Functionality of Pins 47, 48, 50, 51, 52
NO PD RES	NO PD	GPIO Port	Keyboard Scan
10K PD	NO PD	JTAG signals	Keyboard Scan
NO PD	10K PD	GPIO Port	JTAG signals

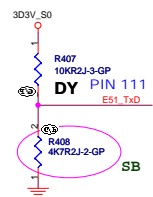
TRIS#(Pin 110) TRI-STATE

Forces the device to float all its output and I/O pins, if an external 10 K Ω pull-down resistor is connected.

BADDR1-0 (PIN 111, 112) I/O Base Address.

10K Ω external pull-down

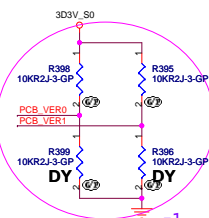
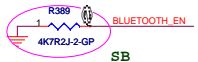
resistor on BADDR1: Core defined



SHBM PIPN83 Shared Host BIOS Memory.

HIGH:NO SHARED(internal resistor)

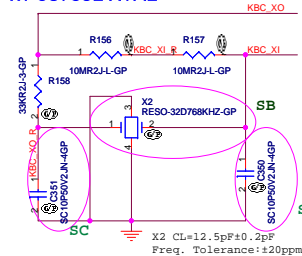
LOW:SHARED BIOS memory.



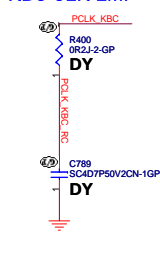
MB VERSION ID

	VER0	VER1
SA	0	0
SB	0	1
SC	1	0
-1	1	1

WPC8763L XTAL



KBC CLK EMI



For Thermal and Capacity button module

21,39,42,44,45,53 PM_SLP_S3#

34 POWER_SW#

18 LCD_CBL_DET#

38 AC_IN#

30 LID_CLOSE#

34 INSTANT_BTN#

21,24 PM_CLKRUN#

37 BAT_IN#

18 BRIGHTNESS

30 CHRG#

36 BATFULL_LED

37 ACDC_ID

36 PWLED

21 PM_PWRBTN#

34_SNRK_LED

29 WLAN_EN

23 HDBG_EN

53 GFX_CORE_ON

34 NUM_LED

34 CAP_LED

34,36 LED_MASK#

30 SNIFFER_BLUE

18 LCD_TST

48 SS_ENABLE

21 KSMRST#_KBC

37 AD_OFF

26 PM_LAN_ENABLE

36 CHARGE_LED

30 CAPA_INT#

34_WLAN_LED_TEST

TPAD28 TP301

37 PSID_DISABLE#

30 WLANBT_BTNR#

18 LCDVDD_TST_EN

50 PANEL_BKEN

24 GB_RST#

For Thermal and Capacity button module

21,39,42,44,45,53 PM_SLP_S3#

34 POWER_SW#

18 LCD_CBL_DET#

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TPAD28 TP301

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24 GB_RST#

24 GB_RST#

24 GB_RST#

24 GB_RST#

24 GB_RST#

24 GB_RST#

24 GB_RST#

For Thermal and Capacity button module

21,39,42,44,45,53 PM_SLP_S3#

34 POWER_SW#

18 LCD_CBL_DET#

38 AC_IN#

30 LID_CLOSE#

34 INSTANT_BTN#

21,24 PM_CLKRUN#

37 BAT_IN#

18 BRIGHTNESS

30 CHRG#

36 BATFULL_LED

37 ACDC_ID

36 PWLED

21 PM_PWRBTN#

34_SNRK_LED

29 WLAN_EN

23 HDBG_EN

53 GFX_CORE_ON

34 NUM_LED

34 CAP_LED

34,36 LED_MASK#

30 SNIFFER_BLUE

18 LCD_TST

48 SS_ENABLE

21 KSMRST#_KBC

37 AD_OFF

26 PM_LAN_ENABLE

36 CHARGE_LED

30 CAPA_INT#

34_WLAN_LED_TEST

TPAD28 TP301

37 PSID_DISABLE#

30 WLANBT_BTNR#

18 LCDVDD_TST_EN

50 PANEL_BKEN

24 GB_RST#

24 GB_RST#

24 GB_RST#

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24 GB_RST#

24 GB_RST#

24 GB_RST#

24 GB_RST#

24 GB_RST#

24 GB_RST#

24 GB_RST#

For Thermal and Capacity button module

21,39,42,44,45,53 PM_SLP_S3#

34 POWER_SW#

18 LCD_CBL_DET#

38 AC_IN#

30 LID_CLOSE#

34 INSTANT_BTN#

21,24 PM_CLKRUN#

37 BAT_IN#

18 BRIGHTNESS

30 CHRG#

36 BATFULL_LED

37 ACDC_ID

36 PWLED

21 PM_PWRBTN#

34_SNRK_LED

29 WLAN_EN

23 HDBG_EN

53 GFX_CORE_ON

34 NUM_LED

34 CAP_LED

34,36 LED_MASK#

30 SNIFFER_BLUE

18 LCD_TST

48 SS_ENABLE

21 KSMRST#_KBC

37 AD_OFF

26 PM_LAN_ENABLE

36 CHARGE_LED

30 CAPA_INT#

34_WLAN_LED_TEST

TPAD28 TP301

37 PSID_DISABLE#

30 WLANBT_BTNR#

18 LCDVDD_TST_EN

50 PANEL_BKEN

24 GB_RST#

24 GB_RST#

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24 GB_RST#

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24 GB_RST#

24 GB_RST#

24 GB_RST#

24 GB_RST#

24 GB_RST#

24 GB_RST#

24 GB_RST#

ADIA:to Charger

ACDC_ID:from Adapter Conn

KBC_PWRBTN#:from power button

BAT_IN#:from Battery Conn

DC_BATFULL#:for Battery charge LED 1

CHARGE_LED#:for Battery charge LED 2

WLAN_TEST#:for WKS test WLAN LED

AD_OFF:enable AC adapter power source

WLAN/BT_BTNR#:from Wlan on/off button

GMCH_BL_ON:Sense The Backlight On/Off Status from VGA Chip

WIRELESS_EN:Disable/Enable Wireless Module

BLUETOOTH_EN:Disable/Enable Bluetooth

USB_PWR_EN#:to on/off USB power switch

AC_IN#:From Charge

GFX CORE ON

R528

S5_ENABLE

R386

R386

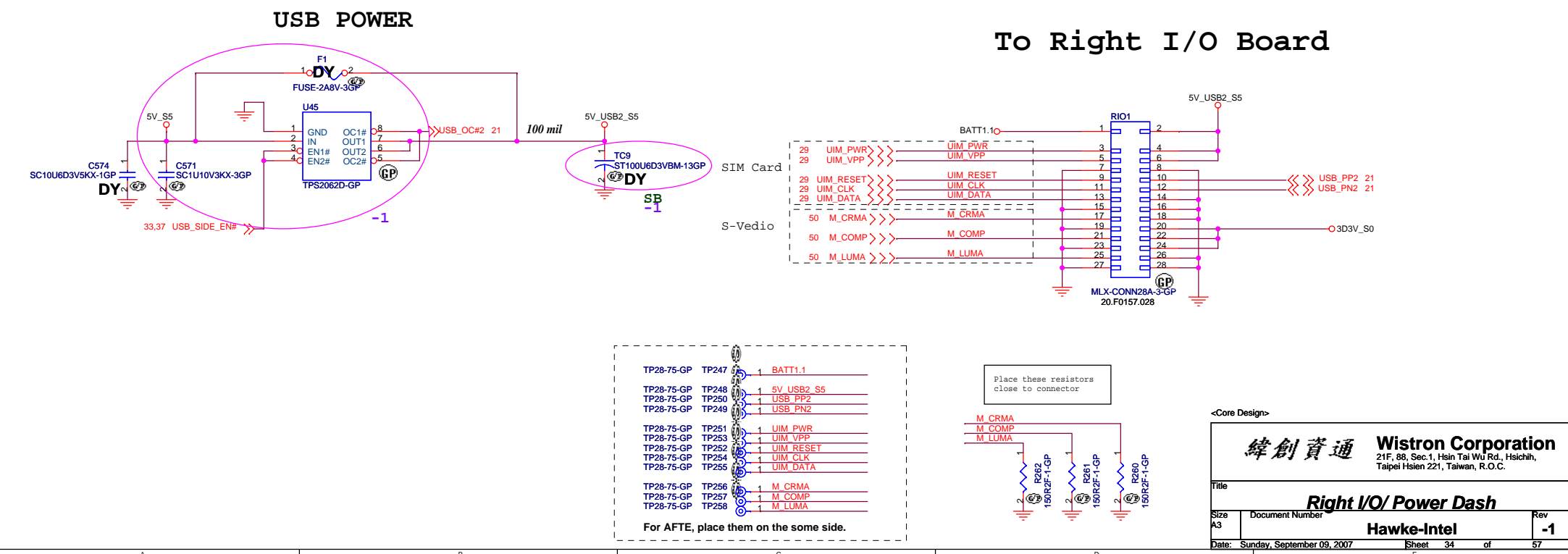
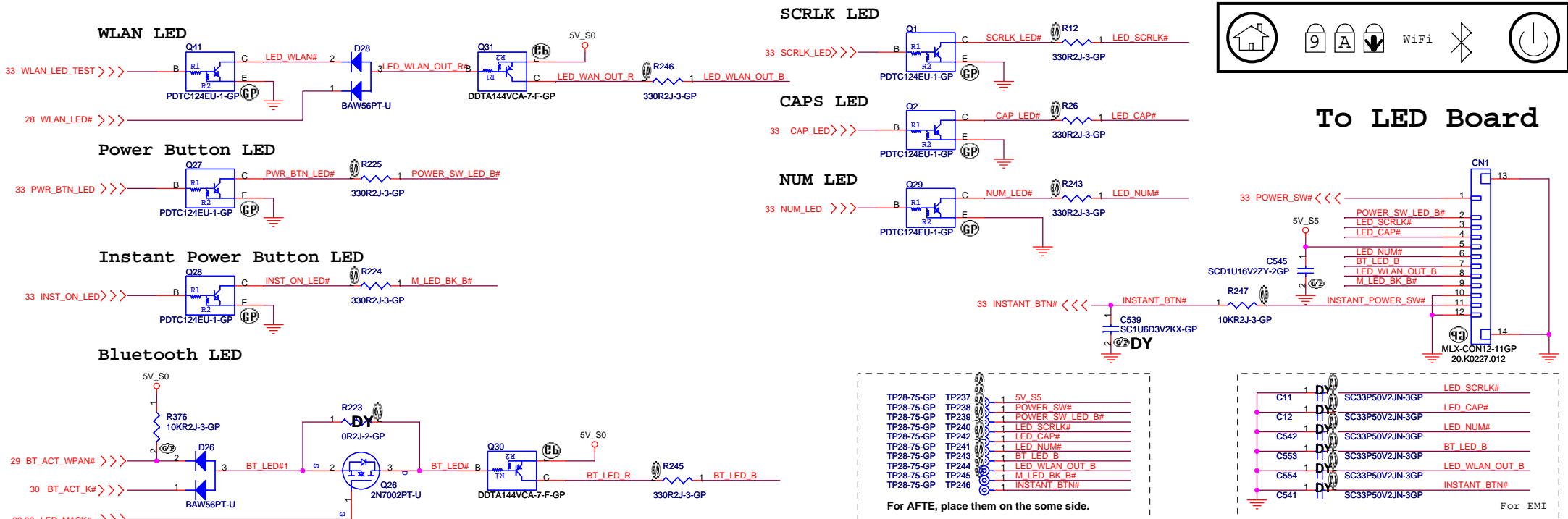
R386

R386

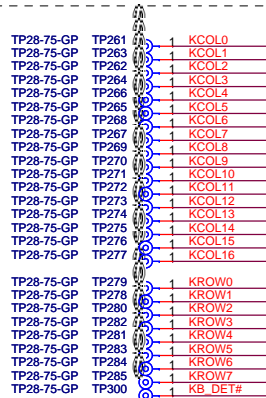
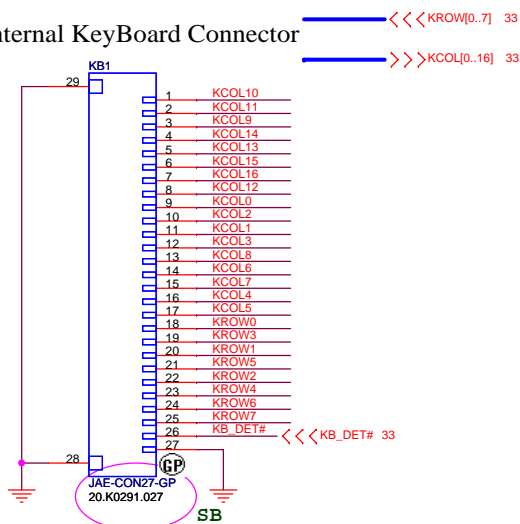
R386

R386

R386

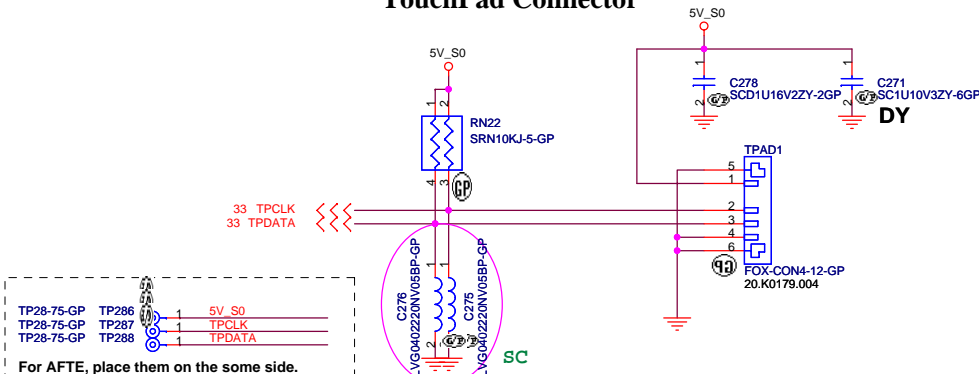


Internal KeyBoard Connector



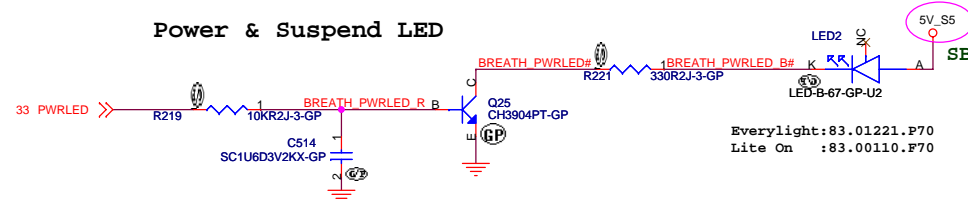
For AFTE, place them on the same side.

TouchPad Connector



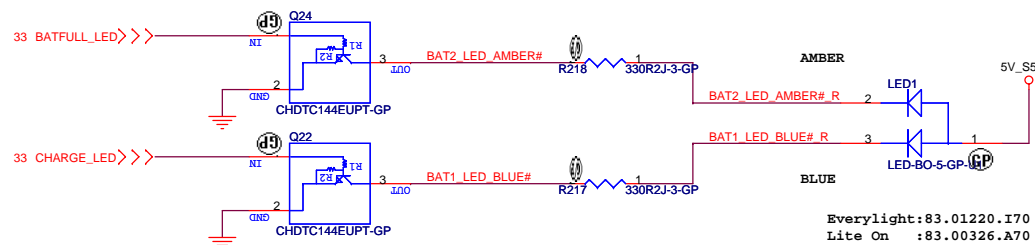
For AFTE, place them on the same side.

Power & Suspend LED



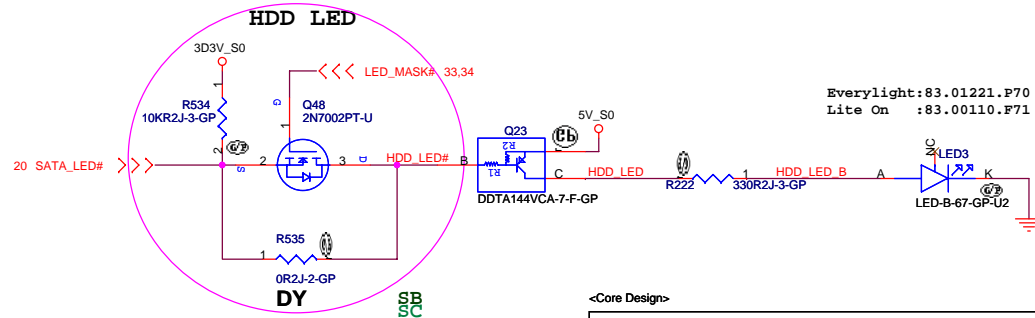
Everylight:83.01221.P70
Lite On :83.00110.F70

Battery LED



Everylight:83.01220.I70
Lite On :83.00326.A70

HDD LED



Everylight:83.01221.P70
Lite On :83.00110.F71

LED Board

LED NAME

ACTIVE SIGNAL

Power Button LED	PWR_BTN_LED	*
Instant Power Button LED	INST_ON_LED	*
WLAN LED	WLAN_LED_TEST (from KBC)	
	WLAN_LED# (from Mini)	
Bluetooth LED	BT_ACT_WPAN# (from Mini)	
	BT_ACT_K# (from BT)	
NUM LED	NUM_LED (from KBC)	
SCRLK LED	SCRLK_LED (from KBC)	
CAPS LED	CAP_LED (from KBC)	

Main Board

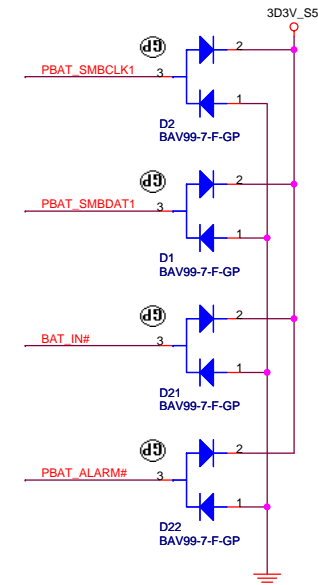
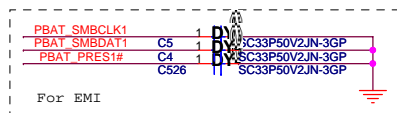
Power & Suspend LED	PWRLED (from KBC)
HDD LED	SATA_LED# (from ICH)
Battery LED	BATFULL_LED (from KBC)
	CHARGE_LED (from KBC)

<Core Design>

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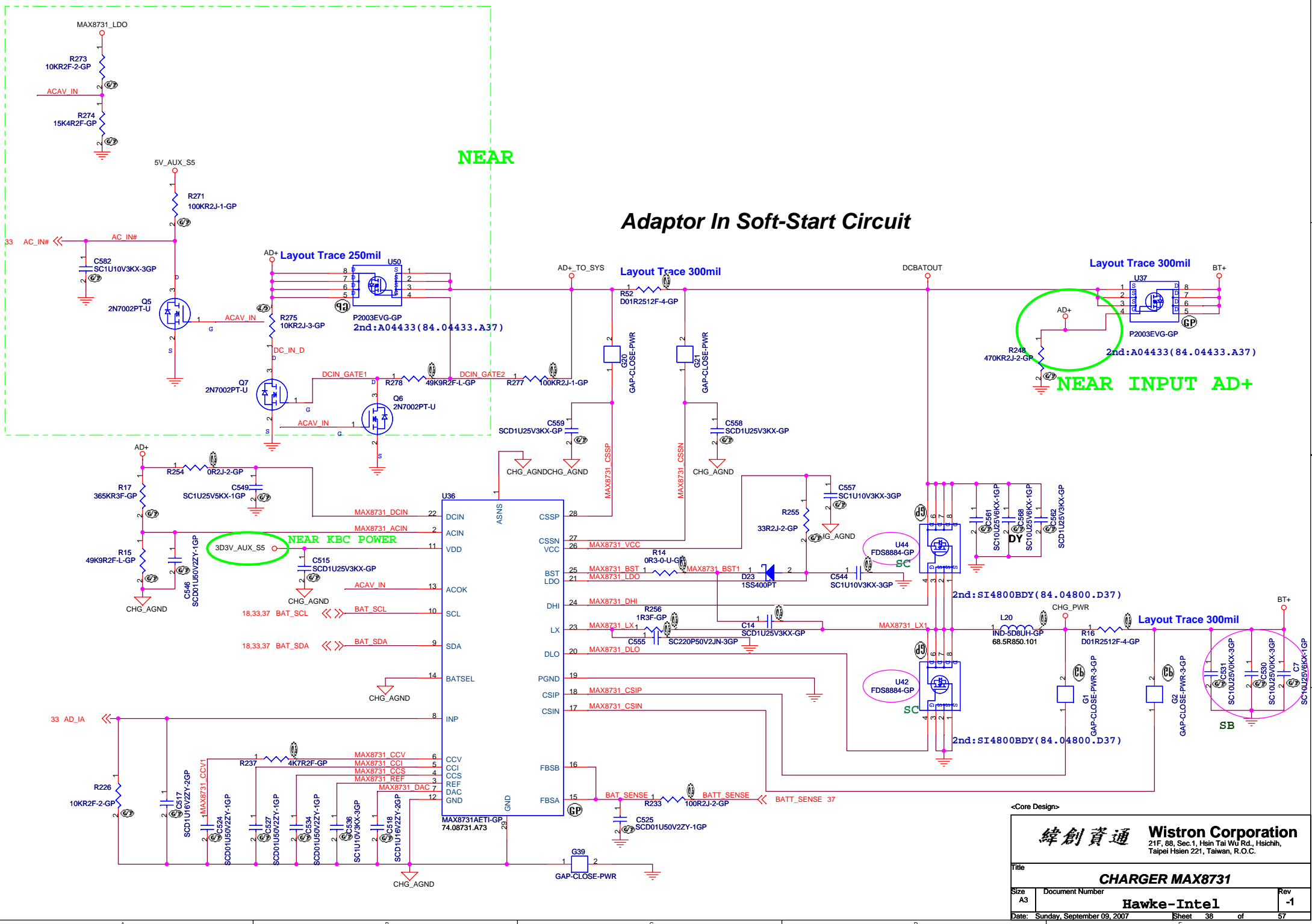
File	KeyBoard/Touchpad	Rev
Size	Document Number	A3
Date:	Sunday, September 09, 2007	Sheet 36 of 57
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**To Left I/O Board
(Adapter In/ USB x 2)**



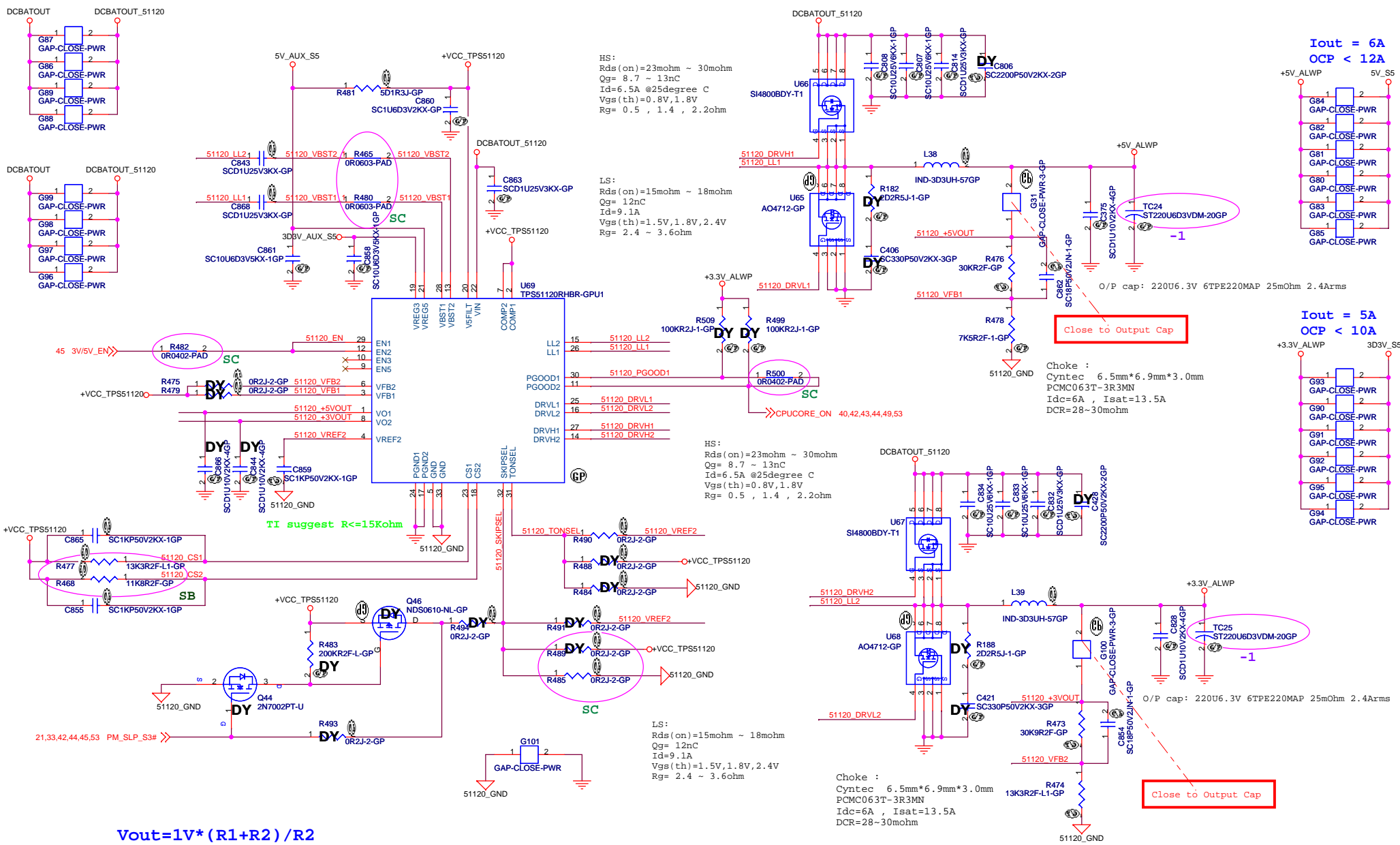
緯創資通 **Wistron Corporation**
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Title			
AD/BATT CONN			
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Adaptor In Soft-Start Circuit

NEAR INPUT AD+



$$V_{out} = 1V \cdot (R1 + R2) / R2$$

	GND	VREF2	FLDLY	VSPILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

<Core Design>

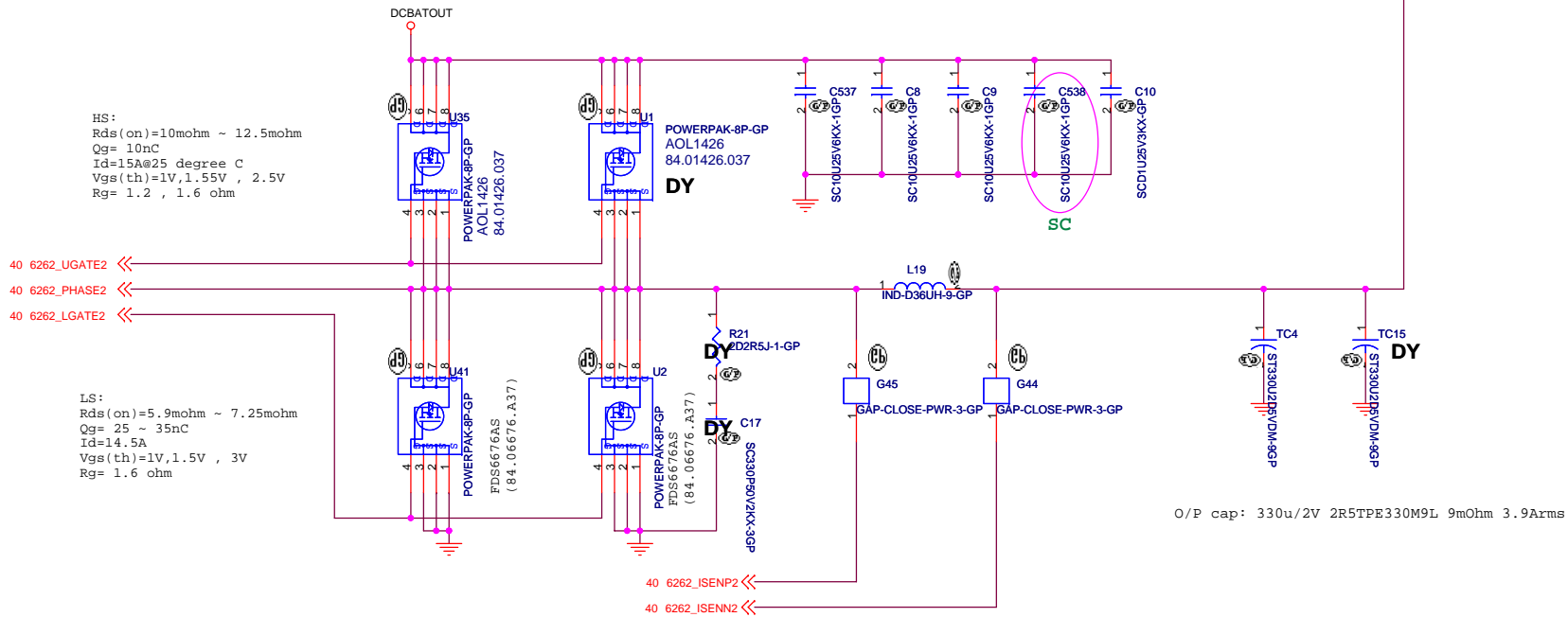
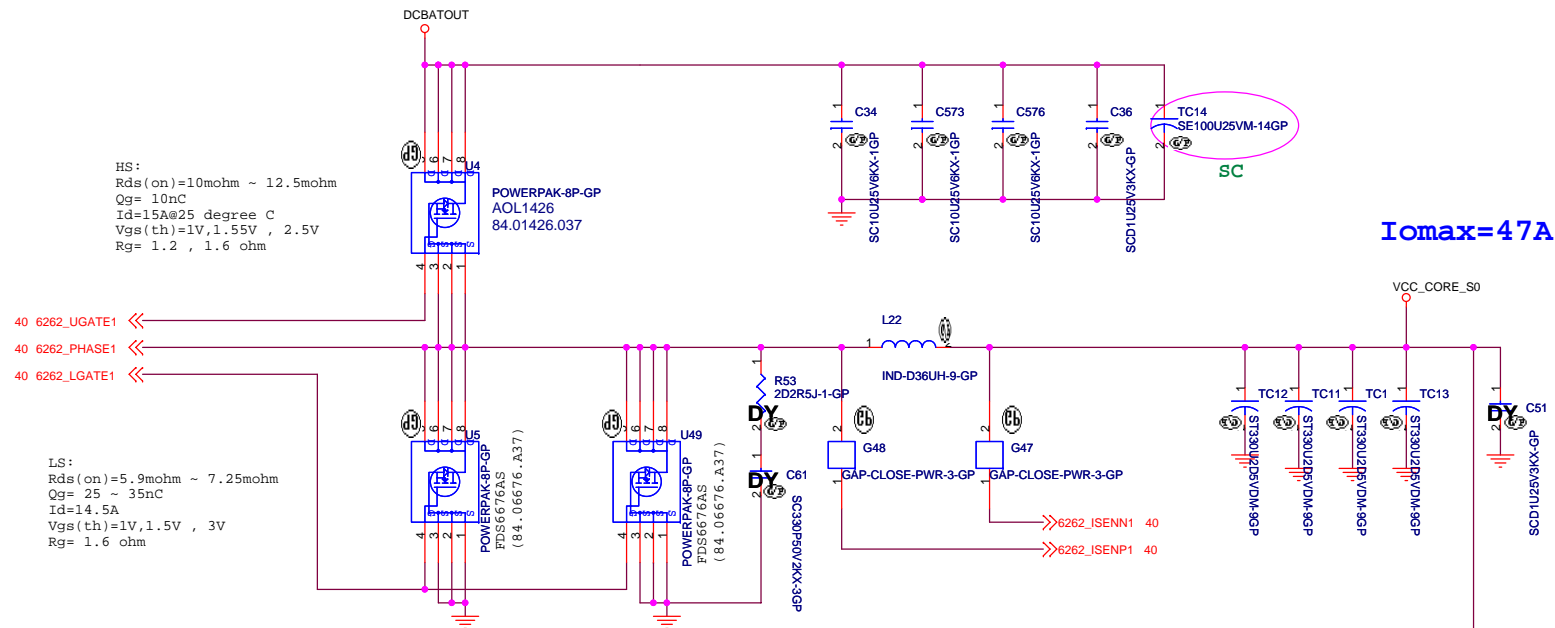
緯創資通 Wistron Corporation
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File: **DC to DC 3.3V & 5V**

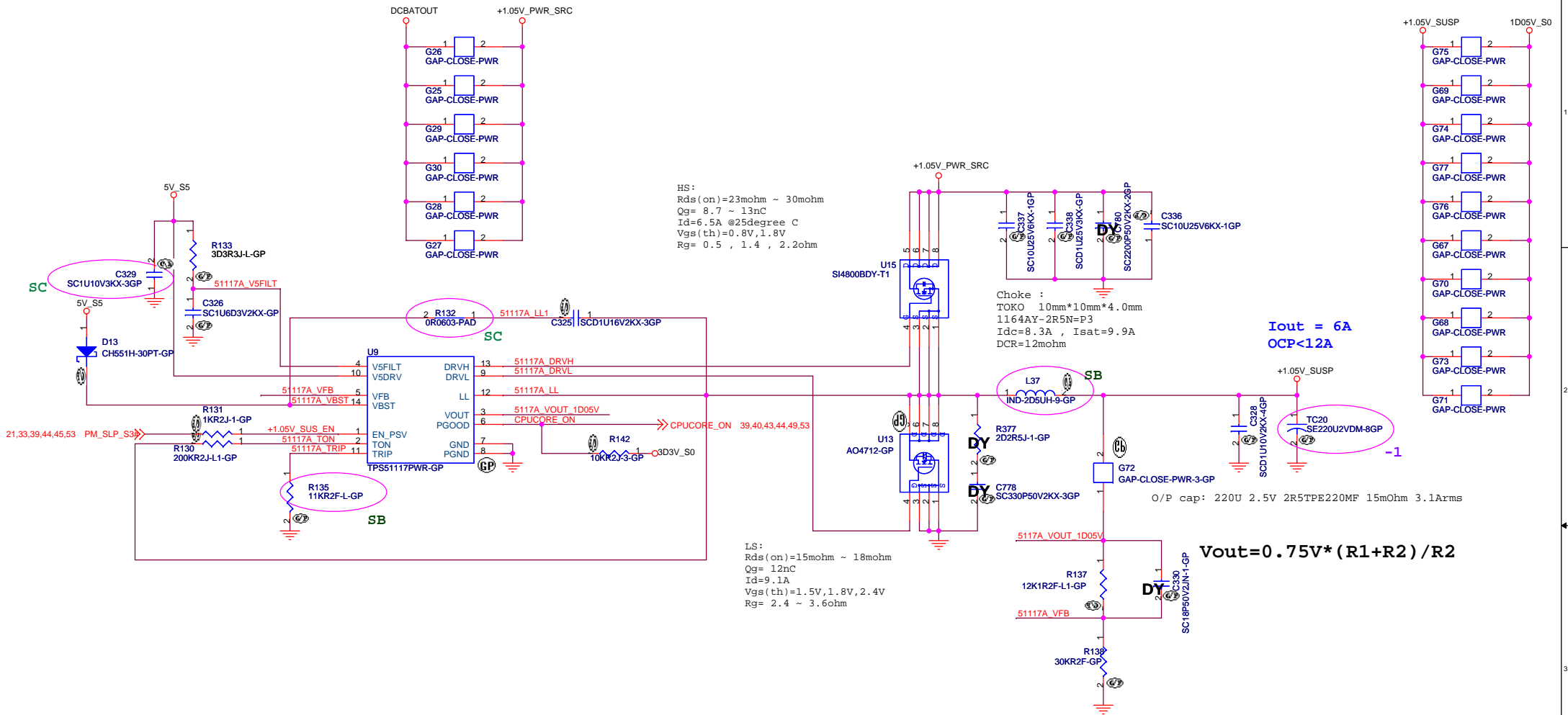
Size: Document Number
Custm: **Hawke-Intel** Rev: **-1**

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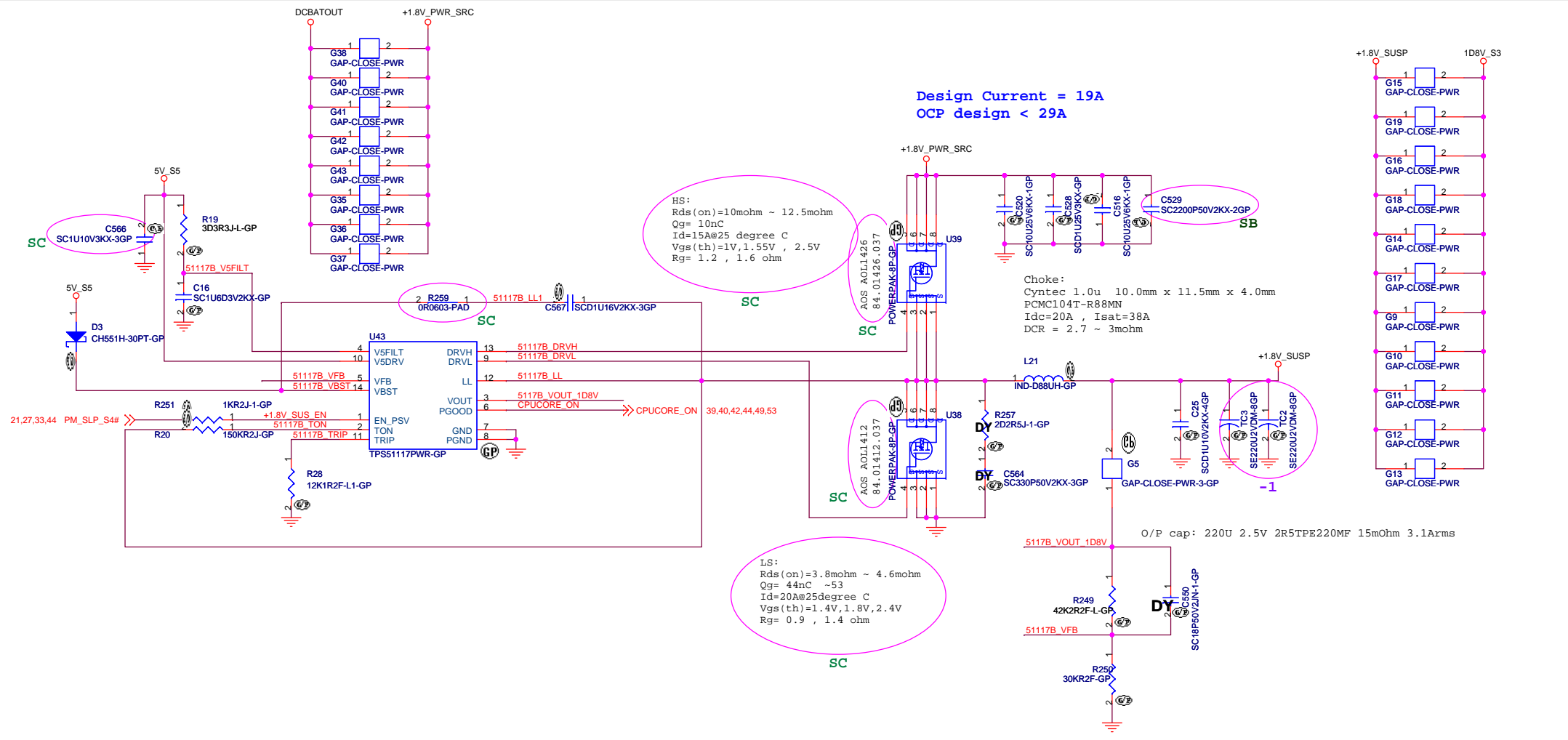
If VCC_SENSE and VSS_SENSE pins have pulled
 resistors to VCC_CORE_S0
 ==> Remove R44/R45/R46/R47.



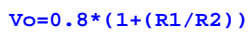
<Core Design>

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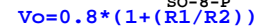
Title			DCDC 1.05V	
Size	Document Number			Rev
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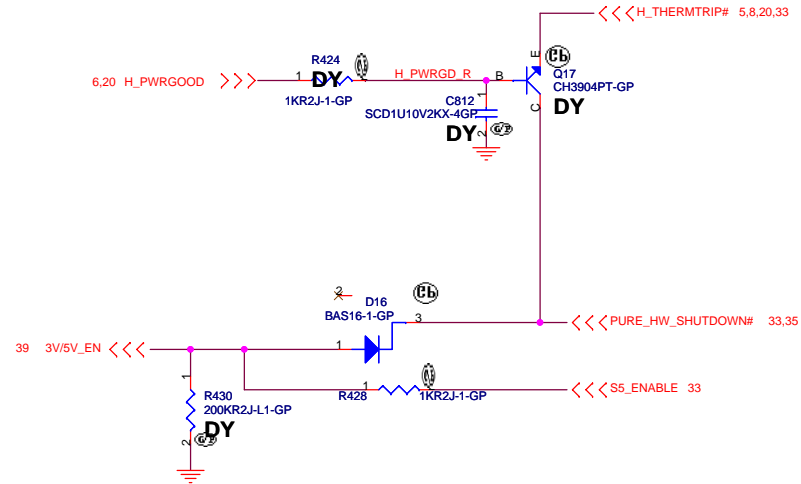
$$V_{out}=0.75V \cdot (R1+R2) / R2$$



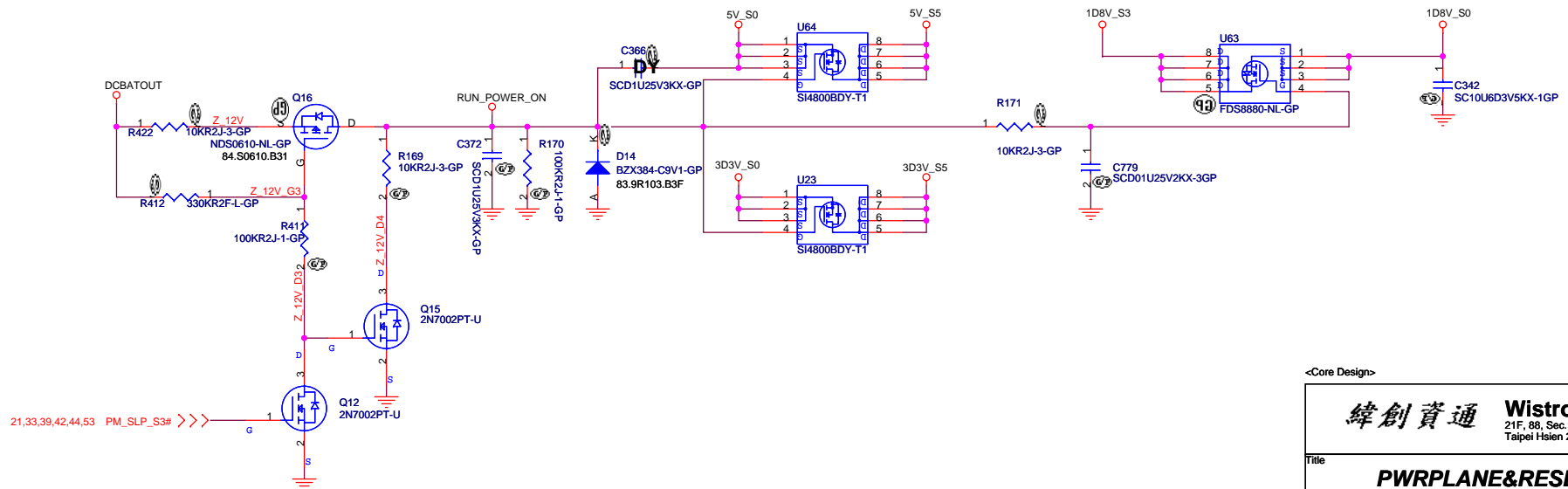
0.9 Volt +/- 5%
Design Current: 1.05A
Peak current 1.5A



Sanyo
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm



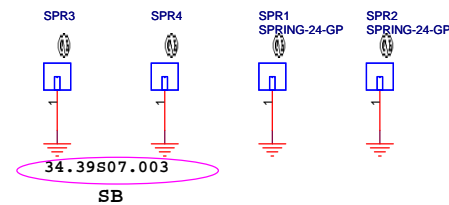
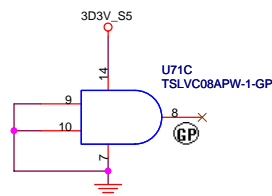
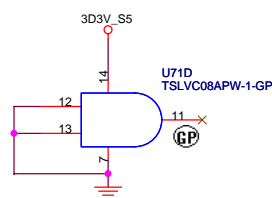
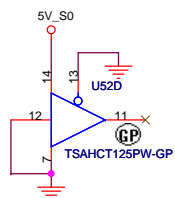
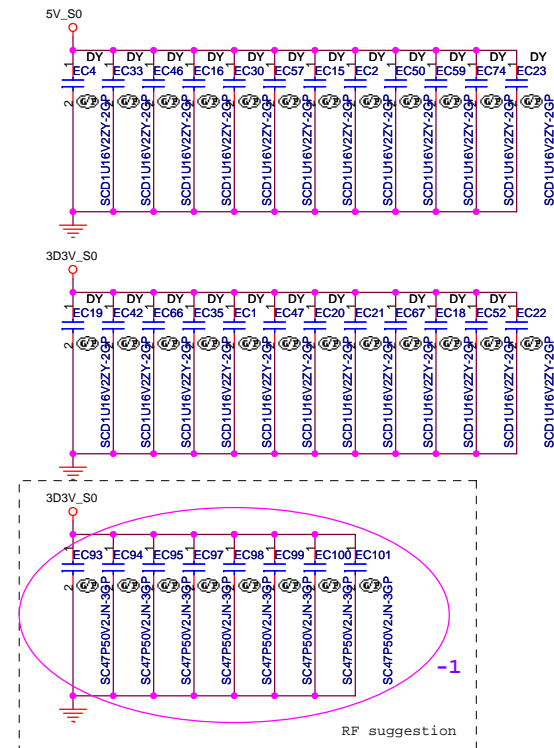
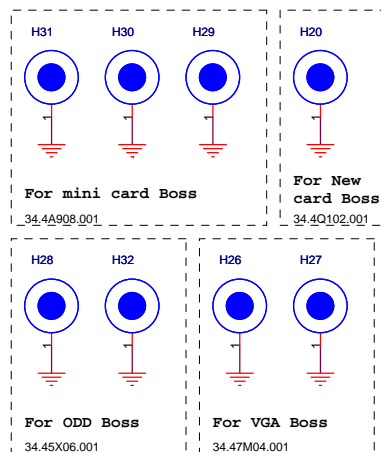
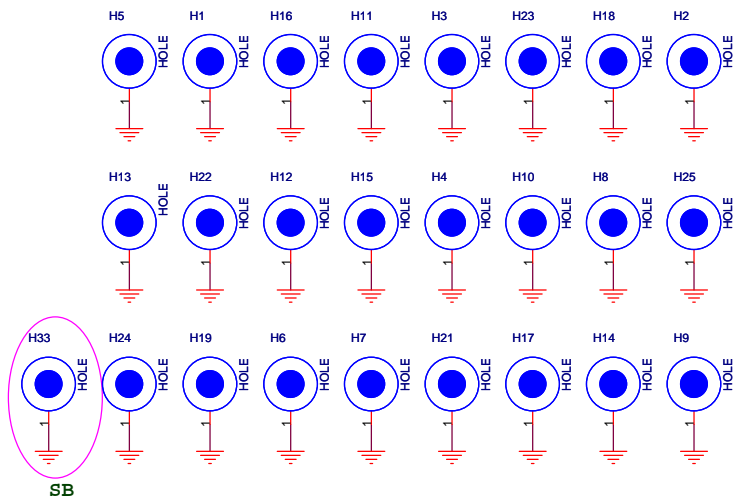
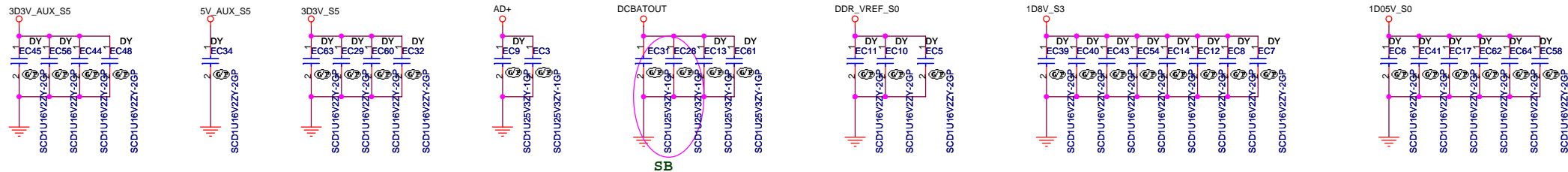
Run Power



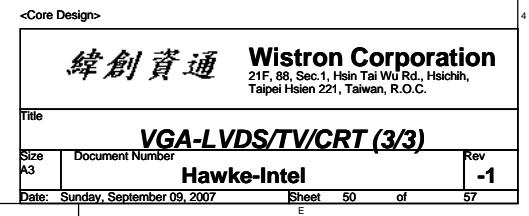
<Core Design>

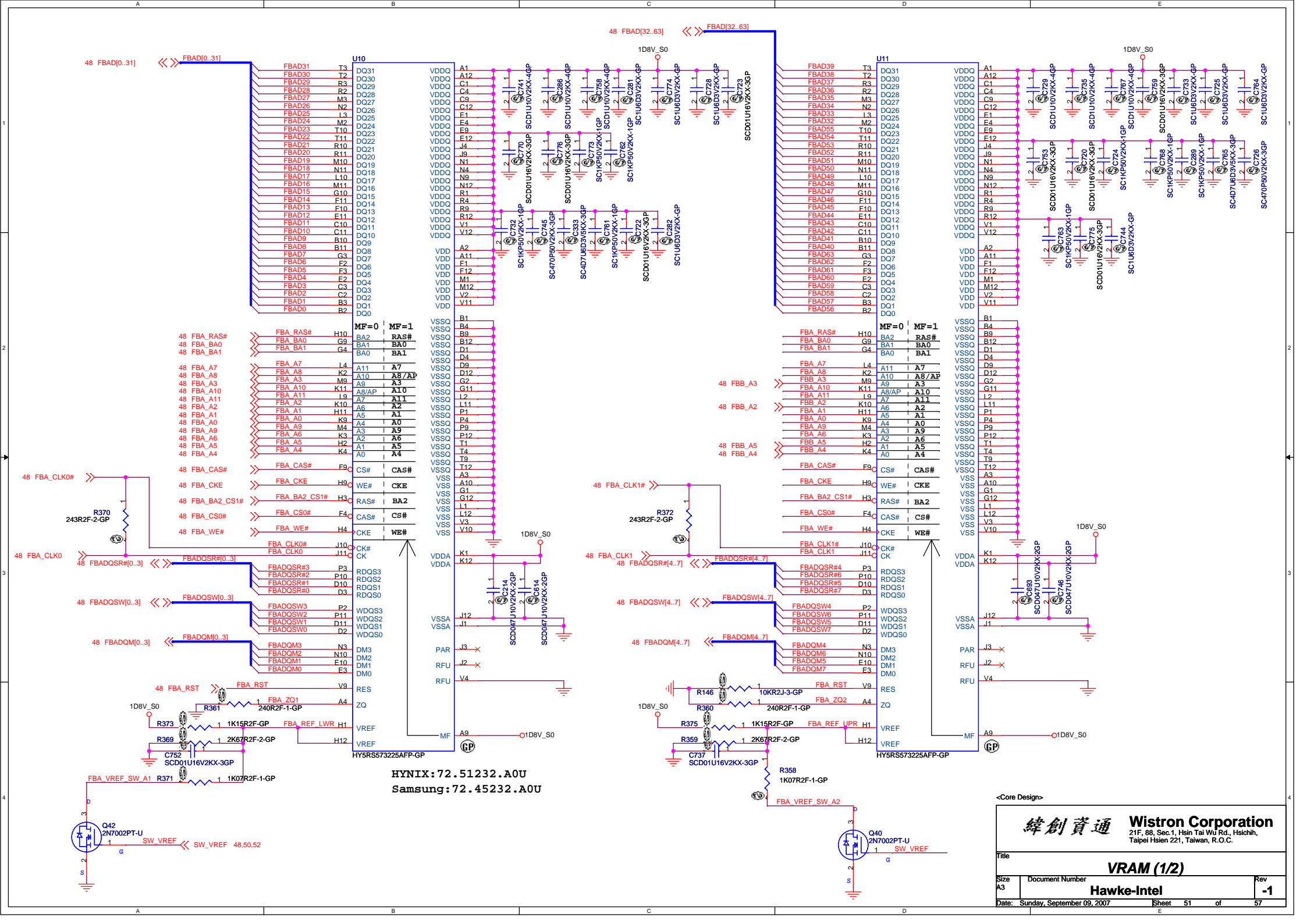
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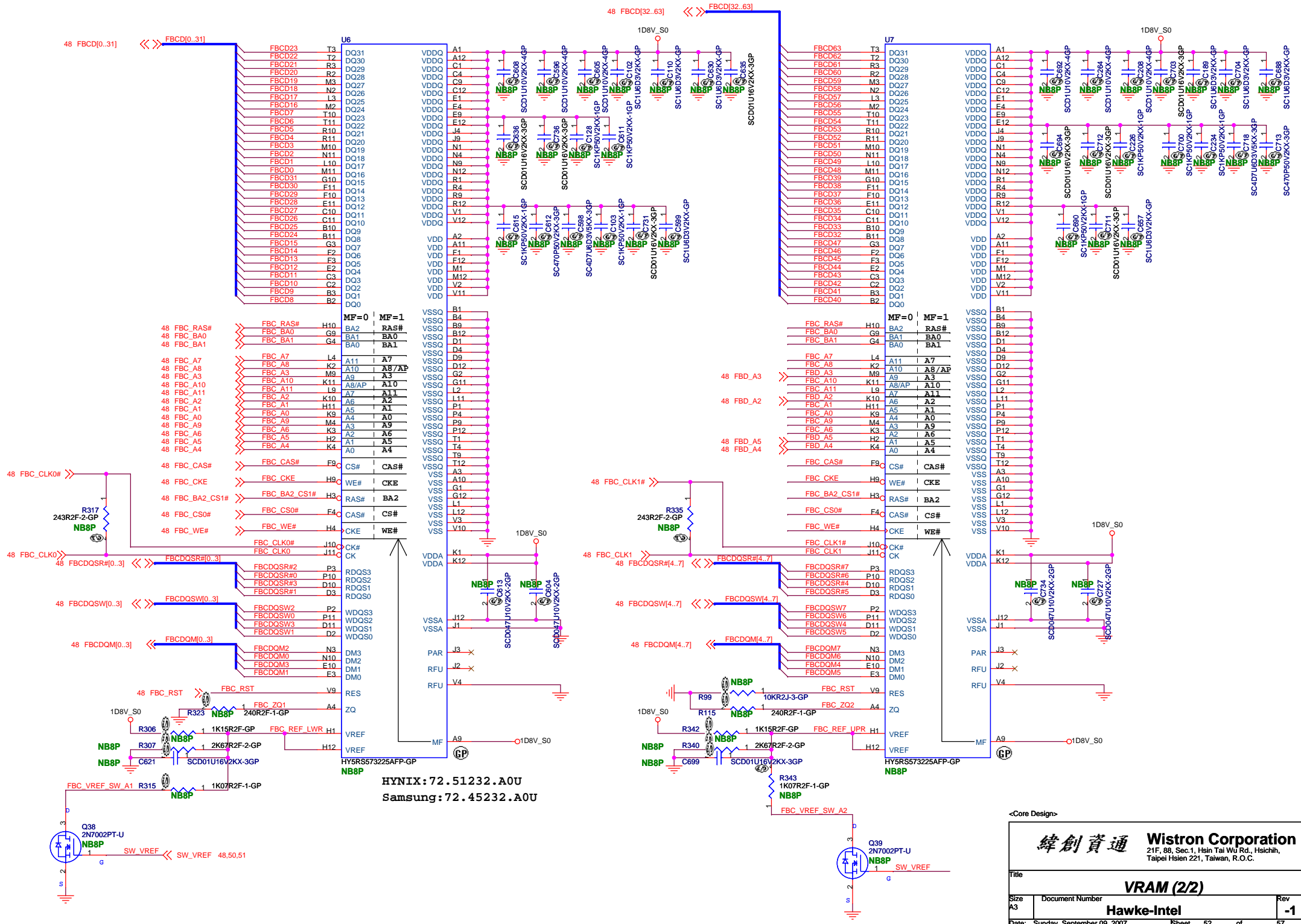
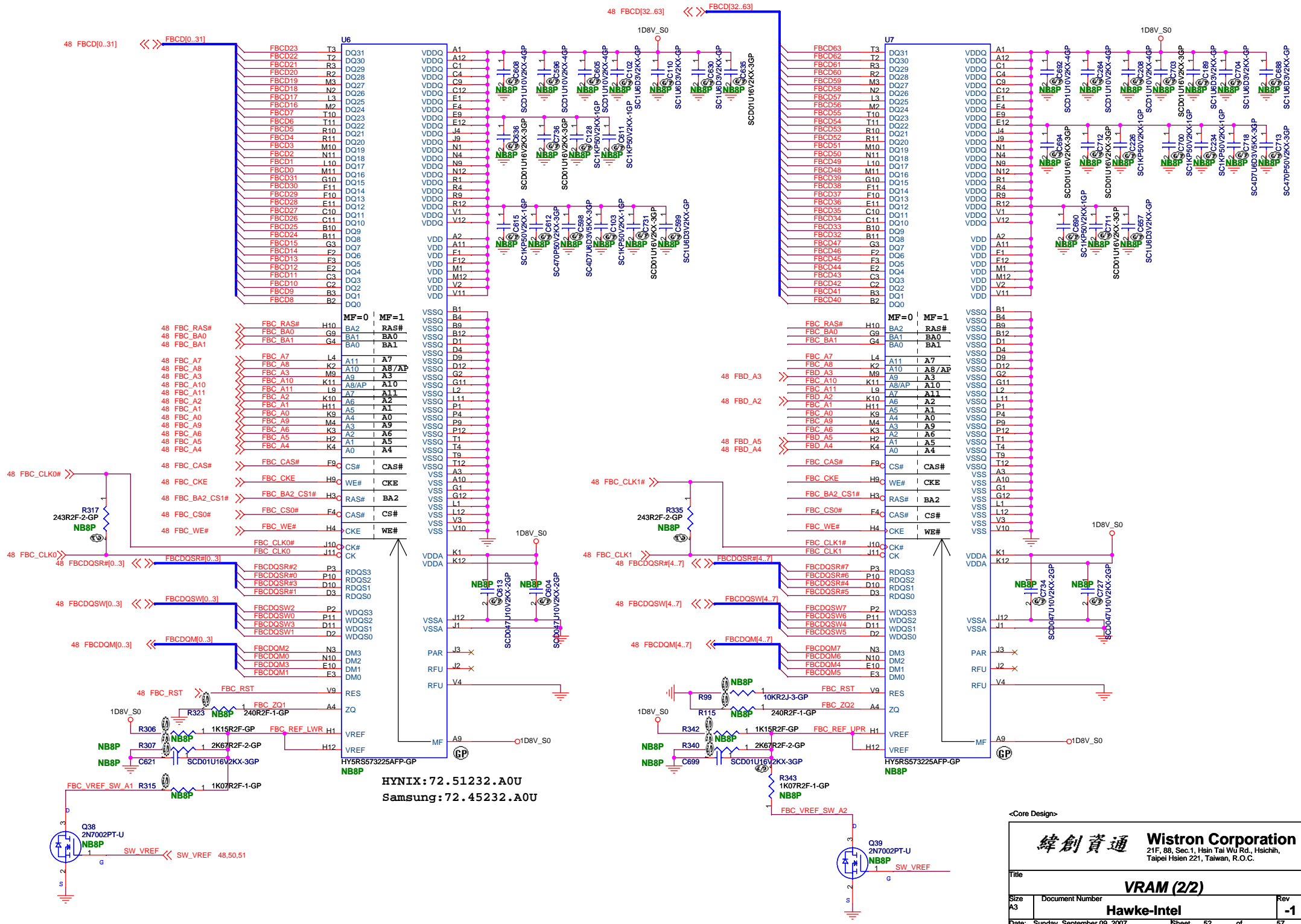
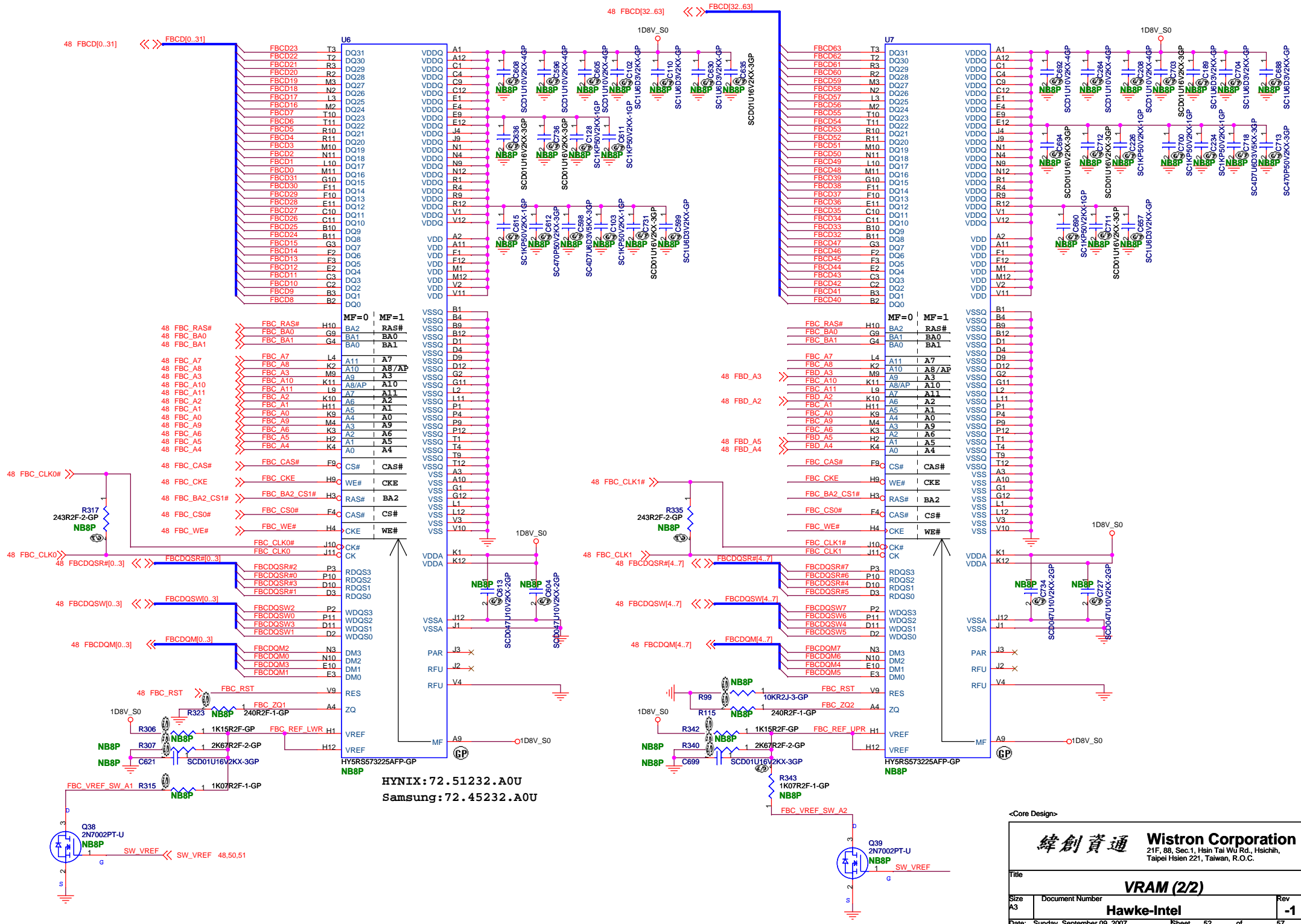
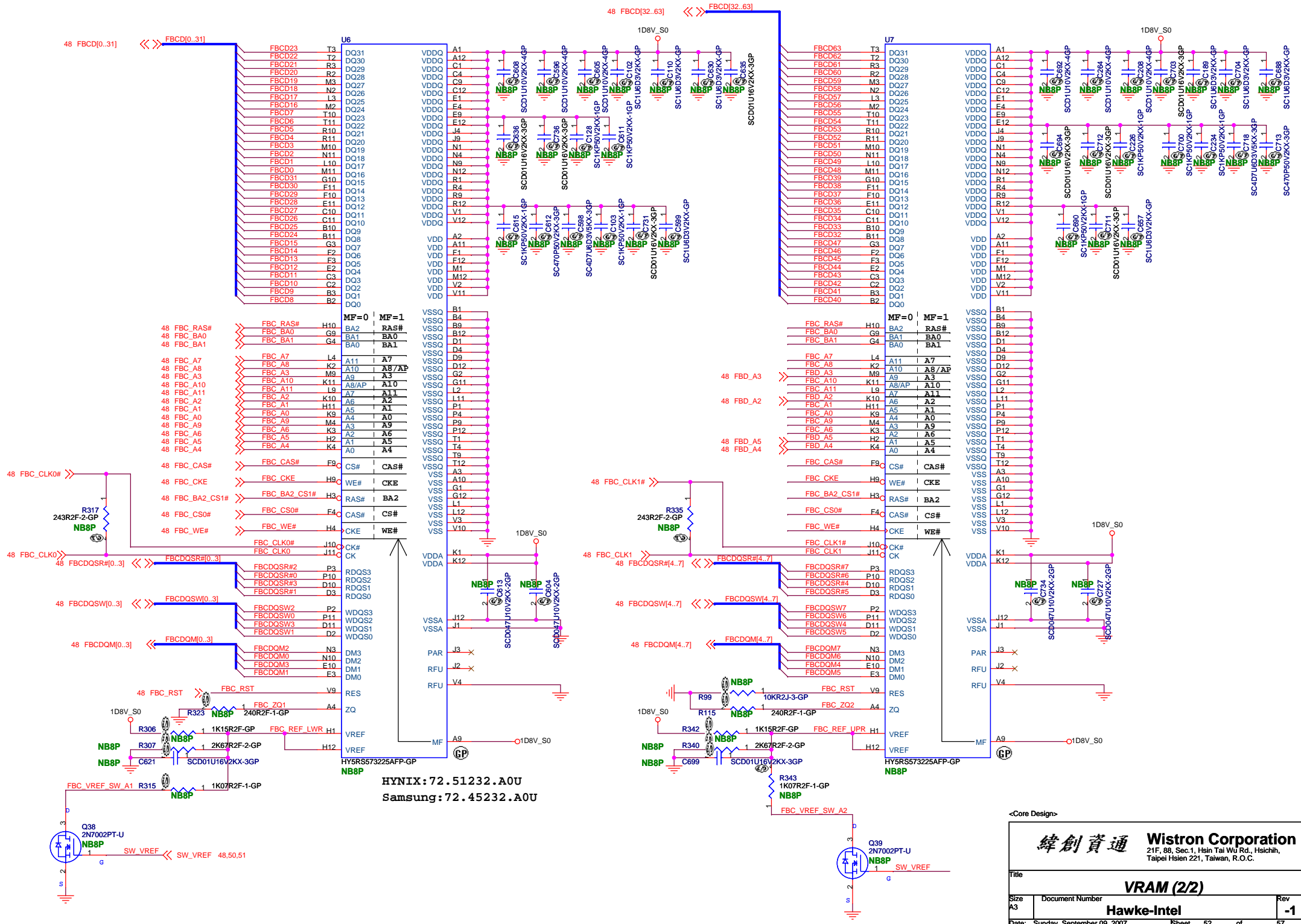
Title		
PWRPLANE&RESETLOGIC		
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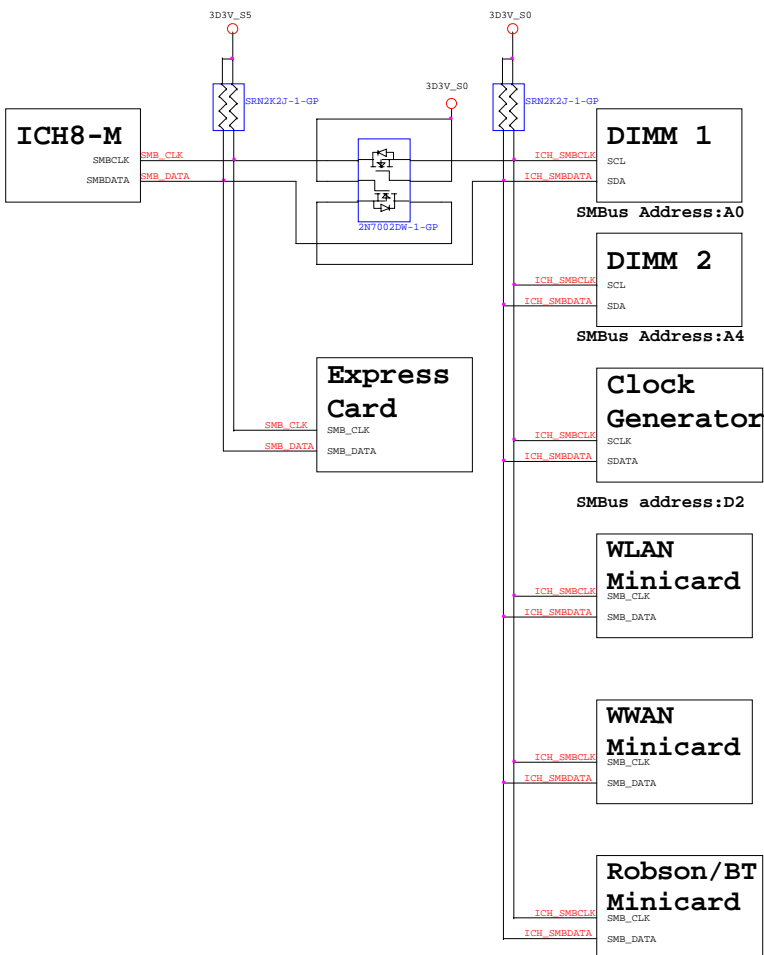




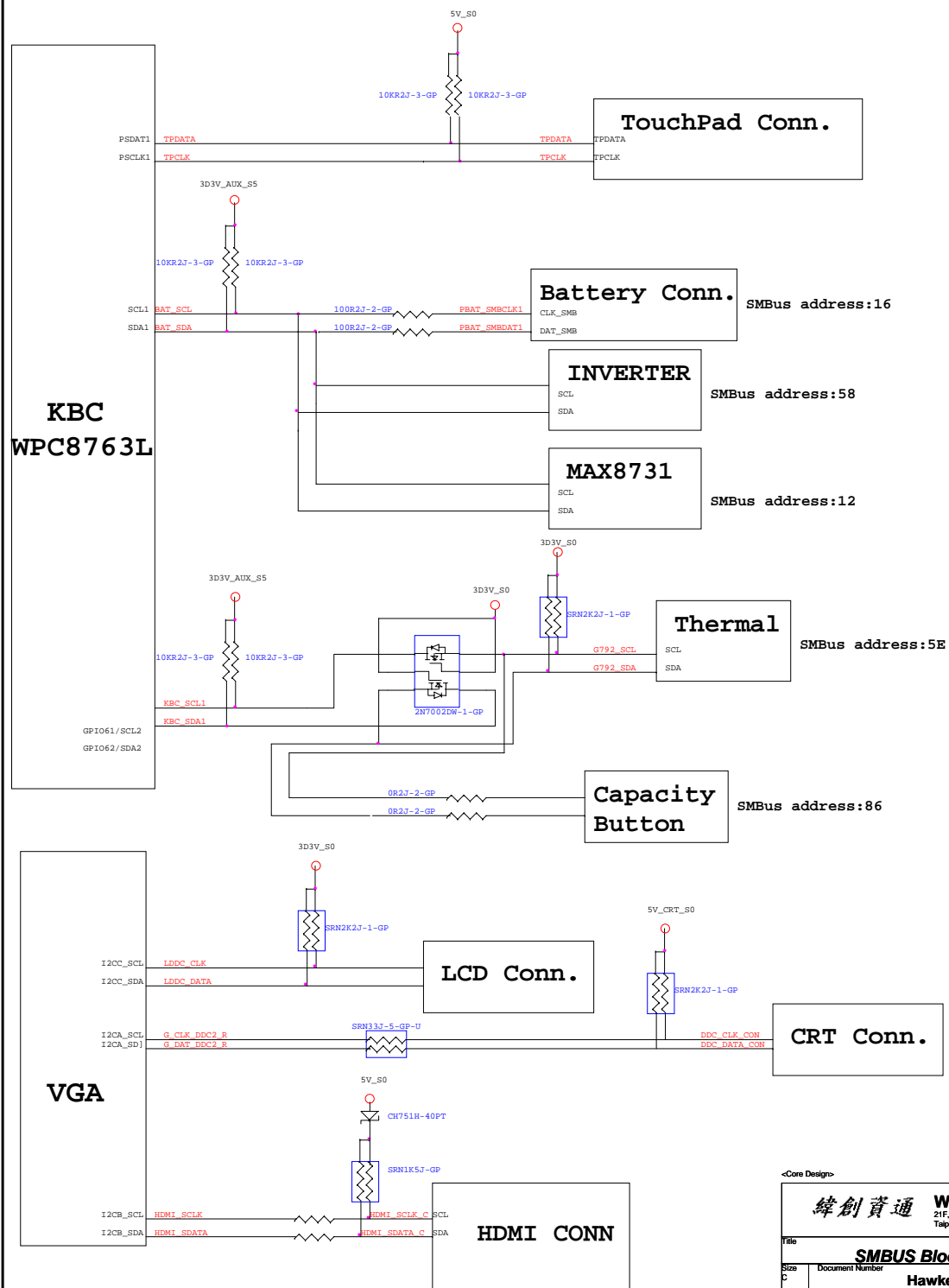




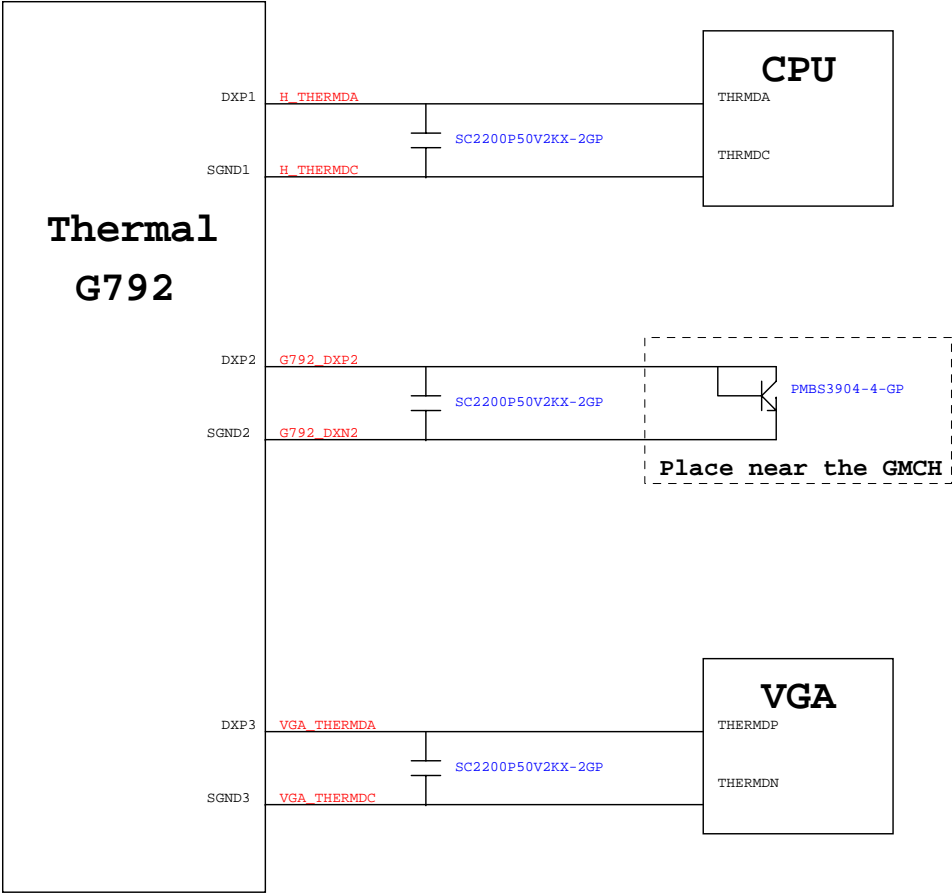
ICH8 SMBus Block Diagram



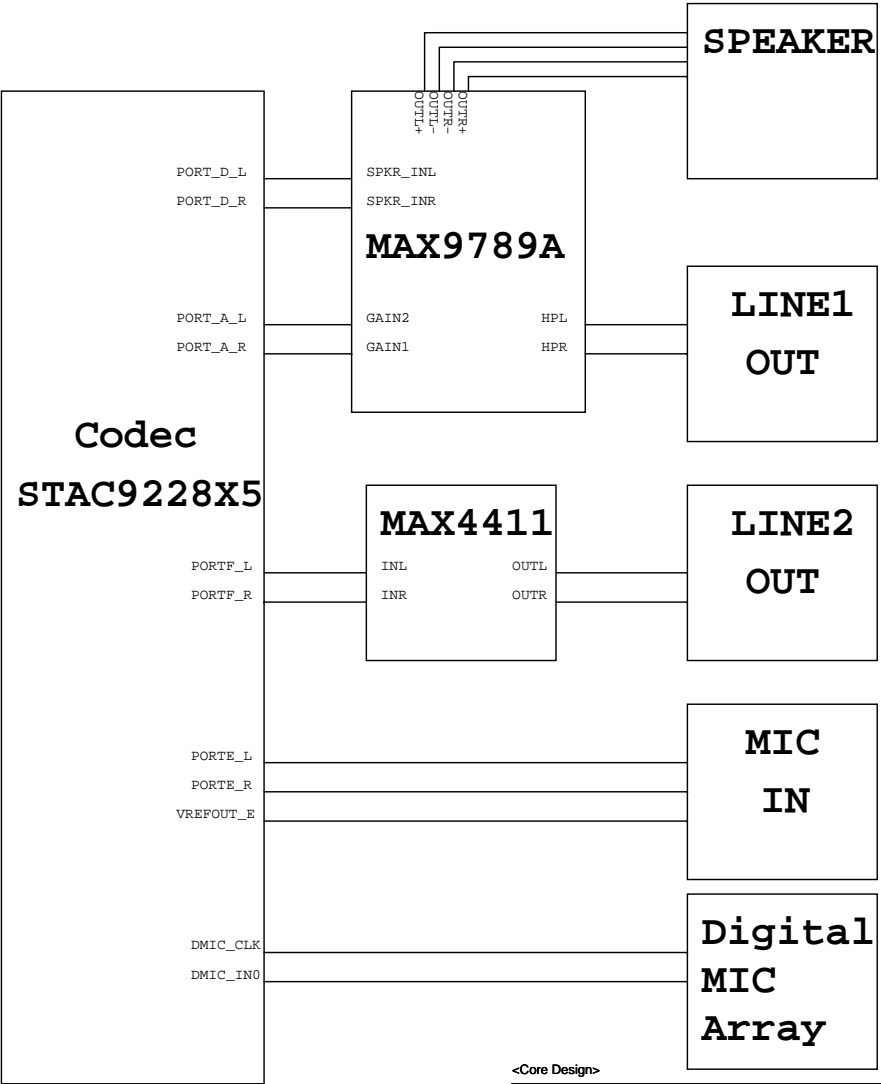
KBC SMBus Block Diagram



Thermal Block Diagram

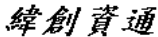


Audio Block Diagram



DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/07/06	X00 to X01	1	4	Changed R431 from 10K ohm to 2.2K ohm.	Follow M08 design.	EE
		2	4	Changed X4's CL from 20pF to 10pF and changed C392 and C399 from 27pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		3	4	Changed RN27, RN28, RN29 and RN31 from 0 ohm to 22 ohm.	To solved these clock signals' Slew Rate are over spec.	EE
		4	18	Changed LVDS connector from 42-pin to 40-pin.	By ME suggestion.	ME
		5	18,33	Connected the LCD1 pin 3 to GND and connected pin 6 to WPC8763's GPIO05 (pin 108 of U17) with 10K ohm pull up to 3D3V_AUX_S5.	Supported the LCD cable PAID.	EE
		6	18	Added EC75-EC78 near CAMERA1.	By EMC team suggestion.	EMC
		7	20	Change C354 and C355 from 15pF to 12pF and changed X1 package from DMX26S to SM-14J.	By the Xtal vendor's FAE suggestion.	EE
		8	21	Added R526 10K ohm between GPIO26 and 3D3V_S0, removed R404.	To solved 3D3V_S0 has leakage when S3 and S5.	EE
		9	21	Added the reserved Q47, D31, R530, R531 and R532.	For test EC_RMRST#_R circuit.	EE
		10	21	Changed R442 from 22.6 ohm to 20 ohm.	To sloved the left side USB ports and Camera USB's eye diagram fail.	EE
		11	23	Changed HDD connector.	By ME suggestion.	ME
		12	25	Changed 1394 connector.	To used reverse type by ME suggestion.	ME
		13	25	Changed X5's CL from 20pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		14	25	Removed R466, U26, R192 and D19, and connected the net MC_PWR_CTRL_0 to U25 pin 4.	For these materials are no used.	EE
		15	25	Populated C887, C888 and C894-C896.	By EMC team suggestion.	EMC
		16	26	Changed C387 and C390 from 27pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		17	27	Changed RJ1 connector.	By ME suggestion.	ME
		18	30	Changed U61 from 8Mbits to 16Mbits SPI ROM.	By customer requirement.	EE
		19	30	Added EC79-EC82 near CAP1.	By EMC team suggestion.	EMC
		20	30	Added EC83-EC88 near BT1.	By EMC team suggestion.	EMC
		21	30	Added EC90-EC91 near CN2 (Biometric).	By EMC team suggestion.	EMC
		22	31	Changed C880 and C881 from 0402 size to 0603 size.	Follow Thurman design.	EE
		23	32	Swaped the nets AUD_HP1_OUT_R1, AUD_HP1_OUT_L1 with AUD_AMP_GAIN1, AUD_AMP_GAIN2.	To sloved the HP1 hadn't output.	EE
		24	32	Changed R211 and R212 from 100K ohm to 10M ohm.	To sloved the AUD_HP1_EN and AUD_HP2_EN volatge level lower than 2V.	EE
		25	33	De-pop R396 and populated R395.	To changed the MB version id to SB.	EE
		26	33	Changed R391 and R405 from 10K ohm to 100K ohm.	To sloved the INSTANT_BTN# and SNIFFER_PWR_SW# can't work.	EE
		27	33	Added R527 100K ohm between WLAN/BT_BTN# and 3D3V_AUX_S5.	To sloved the WLAN/BT_BTN# can't work.	EE
		28	33	Changed X2 package from DMX26S to SM-14J.	By the Xtal vendor's FAE suggestion.	EE
		29	33,36	Changed KB1 from 25-pin to 27-pin connector, connected the KB1 pin 27 to GND and connected pin 26 to WPC8763's GPI92 (pin 99 of U17) with 10K ohm pull up to 3D3V_AUX_S5.	Supported the KB cable PAID.	ME,EE
		30	33	Changed R408 and R389 from 10K ohm to 4.7K ohm.	By Vendor's FAE suggestion.	EE
		31	35	Changed FAN1 from 4-pin to 3-pin connector.	By ME suggestion.	ME
		32	36	Added R534, Q48 and R535 off SATA_LED# and Q23.	Supported the HDD LED is dim when sinffer switch press.	EE
		33	36	Connected LED2 pin A from 5V_S0 to 5V_S5.	To sloved the Power LED can't breath when system enter S3.	EE
		34	38	Changed C530 and C531 from 1206 size to 1210 size and populated C7.	To solved noise when battery full load.	Power
		35	39	Changed R477 from 12.1K ohm to 13.3K ohm and changed R468 from 12.1K ohm to 11.8K ohm.	To adjust 3.3V and 5V current limit by power team suggestion.	Power
		36	40	Changed R7 from 12.7K ohm to 11.8K ohm and changed R468 from 3.24K ohm to 3.65K ohm.	To adjust CPU Vcore current limit by power team suggestion.	Power
		37	42	Changed R135 from 12.1K ohm to 11K ohm .	To adjust 1.05V current limit by power team suggestion.	Power
		38	43	Populated C529.	By EMC team suggestion.	EMC
		39	46	Added more one hole H33.	By EMC team suggestion.	EMC
		40	46	Populated EC28 and EC31.	By EMC team suggestion.	EMC
		41	47	Added C900, C901, C904 10uF and TC26 100uF.	To sloved VGA Vcore had OVP when run 3Dmark.	Power
		42	53	Changed R135 from 12.1K ohm to 10.5K ohm .	To adjust CPU Vcore current limit by power team suggestion.	Power
		43	53	Added EC89 0.1uF between DCBATOUT and GND.	By EMC team suggestion.	EMC

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Title	
HISTORY from X00 to X01	
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DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/08/17	X01 to X02	1	4	Changed U22 from ICS 9LPRS365BKLT to Realtek RTM875M-606-LF.	Changed clock gen symbol from ICS 9LPRS365BKLT to Realtek RTM875M-606-LF.	EE
		2	15	Changed HDMI power rail from +5V_HDMI to 5V_S0.	Follow Thurman design.	EE
		3	17	Populated D4, D5, D6, D7 and D8.	By NV GPU ESD requirement.	EMC
		4	17	Changed L1, L2 and L4 from BLM18BA100SN1 to BLM18BB470SN1	To solve the ring on RGB singnal.	EE
		5	18,33	Added D32, connected pin 1 to LCDVDD_TST_EN, pin 2 to LCDVDD_EN and pin 3 to ENVDD. Changed R276 from 0 to 100k ohm and changed R276.1 to GND	Added LCDVDD_TST_EN from U17.27 to control U53.3	EE
		6	18	Disconnted LCD1 pin 3 and pin 10	To prevent the power short to GND.	EE
		7	21	Added R542 for ECSCI# need to pull up 3D3V_S0	To solve one of CPU core always loading 100%.	EE
		8	27	Added EC92 22pF between NEWCARD_CLKREQ# and GND	By EMC team suggestion.	EE
		9	27	Added note for transformer source part number.	By EMC team suggestion.	EE
		10	29	1.Changed D20 to U73 for Bluetooth Action circuit. 2.Reserved U73, R193 and R195, populated R194.	1.It can be used both BT module and BT mini-card. 2.Just keep BT module now.	EE
		11	29, 33	Connect MINI2 pin 20 to U17.24 (GPO47 of KBC).	Changed WWAN enable WiFi RF controlled by another GPIO pin (U17.24 is GPO47 of KBC).	EE
		12	30, 33	Rename SNIFFER_YELLOW# to SNIFFER_YELLOW, SNIFFER_BLUE# to SNIFFER_BLUE.	These pins are High active.	EE
		13	30	Disconnted SNIFFER_BD1 pin 8 and CAP1 pin 7.	To prevent power short to GND.	EE
		14	30	Changed EC90 and EC91 from 22pF to MLVG0402220NV05BP.	By EMC team suggestion.	EMC
		15	32	Populated EC24, EC25, EC26 and EC27 and change to 1000pF.	By EMC team suggestion.	EMC
		16	32	Changed Q45 to U47 and added R543.	To add AUD_SPK_ENABLE# controlled by AMP_MUTE#.	EE
		17	32	Changed R197 from 0 ohm to 100K ohm and pull up to +5V_SPK_AMP, dispopulated R505 and populated R213.	To solve HP1, HP2 and Speaker have "BoBo" noisy when power on, off, enter S3.	EE
		18	33	Populated R396 and R398, dispopulated R395 and R399.	Change Board ID to version SC.	EE
		19	36	Populated Q48 and R534, dispopulated R535.	HDD LED should be dim when power on by Sniffer button.	EE
		20	36	Changed C275 and C276 from reserved 33pF to MLVG0402220NV05BP, and populated them	By EMC team suggestion.	EMC
		21	36	Changed KB EMI caps from 220pF to 180pF.	To solved the word has repeat symptom when key-in.	EE
		22	38	The U42 and U44 were swap the main source and 2nd source.	To prevented used AO4468 that SI4800BDY 2nd source on charger H/S and L/S MOS.	EE
		23	39	Populated R485 and dispopulated R489.	To changed 3V and 5V PWM to Skip mode.	EE
		24	42, 43, 53	Changed C329, C566 and C272 rated voltage from 6.3V to 10V.	For derating issues by power team requirment.	EE
		25	43, 53	Change the U56 and U39 from 2nd source to main source, and swap the U38 and U58's the main source and 2nd source	To combined U39 and U56 material item of BOM with CPU H/S MOS (U4 and U35).	EE
		26	20	Changed C354 and C355 from 12pF to 8.2pF.	For Negative Resistance of X1 isn't enough.	EE
		27	33	Changed C350 and C351 from 15pF to 10pF.	For Negative Resistance of X2 isn't enough.	EE

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Title

HISTORY from X01 to X02

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